1 GHz Programmable Analog Phase Shifter for Adaptive Antennas

by

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A thesis submitted in conformity with the requirements
for the degree of Master of Applied Science
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Univeristy of Toronto

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Abstract

Adaptive antennas are currently being considered as a means to improve spectral efficiency of wireless networks. They can be used to spatially separate different mobile user, by forming radiation pattern nulls at the interfering signals. However, the relatively high cost of adaptive antenna systems compared to non-adaptive antennas has hampered their commercial application. The purpose of this thesis is to investigate the feasibility of realizing an integrated circuit that will implement a one GHz programmable analog phase shifter, an important building block of adaptive antenna systems. This could lower the system's cost of adaptive antennas. The programmable analog phase shifter is comprised of a 90^{o} phase shifter, a variable gain amplifier, a summer and a digital-to-analog converter. The resulting chip area is small enough to allow 16 complete phase shifter circuits to be included in a single package, thereby allowing control of an array of 16 antenna elements.

Acknowledgements

I would like to thank my thesis supervisor, Prof. Ken Martin, for his guidance and encouragements during course of my graduate study.

To Gregory Hartman for his valuable suggestions and interesting discussions. To Stephen Alie and Wynstan Tong , for their helpful suggestions in improving Ballistic, which saved me a lot of layout time.

Thanks also goes to Steve Jantzi, Khoman Phang, Bryn Owen and Bob Richens and to the people in ea104.

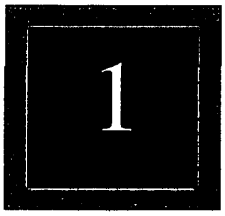
To Jaro Pristupa for helping me with my DRC errors. To Prof. John Long and Leesa Macleod for helping me with the TDR measurements. To Gerald Dubios for his assistance with the network analyzer measurements.

To my brother Arthur and to my family for their patience and support throughout my academic career.

Table of Contents

CHAPTER

Introduction



Phase shifters are commonly found in microwave subsystems. They can be mechanical or electronic, fixed or variable. This chapter gives an overview of electronically variable phase shifters. One of the popular applications of microwave variable phase shifters are in phased-array radars, where inertialess scanning of the radar beam is possible. They are also used as microwave frequency translators, which shift the frequency of a signal by a desired amount. A lossless phase shifter having linear phase variation in time can operate as an ideal frequency translator [KOUL, 91], as shown in figure 1.1(a). The waveform $\phi(t)$ is shown in figure 1.1(b). $\phi(t)$ can also be a periodic sawtooth waveform, as shown in figure 1.1(c), since a sinusoidal function is periodic. The output of figure 1.1(a) can be written as $y(t)= \sin[2\pi(f_o + f_d)t]$, where $(f_o + f_d)$ is the new shifted frequency and $f_d=1/T$. The circuit can also be used in wireless transmitters, where the carrier's magnitude and phase are directly controlled at the carrier frequency. This can be used to realize an almost completely-digital wireless transmitter. Another application is in adaptive antennas (discussed in chapter 2), which are gaining a lot of attention in cellular systems

recently, because of their potential to help satisfy the following needs of cellular systems. They allow for :

- Increased user capacity- The system should be able to serve thousands of clients in a local area.
- Efficient spectrum utilization- Frequency channels should be re-usable in geographically separate cell sites.
- Adaptability to traffic density- The system should be capable of increasing capacity as the traffic density increases in a cellular coverage.

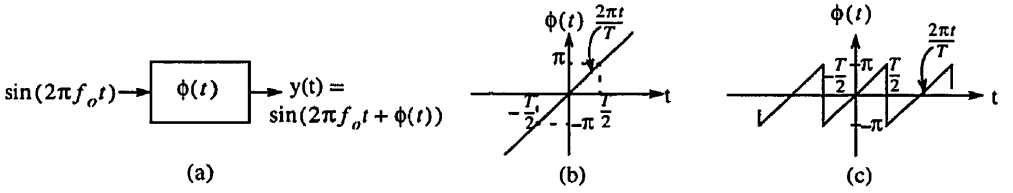


Figure 1.1 Frequency Translator

Advances in variable phase shifters are attributed to the development of phased-array radars, which are used extensively in military applications. This chapter discusses some of the commonly used technique to realize microwave and millimeter-wave phase shifters.

1.1 Phase-Shifter Circuits using Switching Device

This section presents some transmission-type and reflection-type phase shifter circuits. A schematic of a series-mounted transmission-type phase shifting network is shown in figure 1.2. Phase shift results from switching the transmission of the RF signal into two different electrical paths. Among the different implementations are the use of lumped and distributed components to realize the network. Advances in GaAs technology, have allowed these circuits to be realized in monolithic form. The common devices that are used

as switches are the p-i-n diodes and metal-semiconductor field effect transistors (MES-FETs). Figure 1.3 shows the p-i-n diode and FET being used as series and shunt switches.

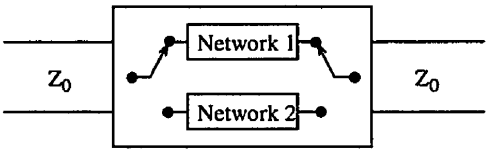


Figure 1.2 Schematic of Transmission-type phase shifter

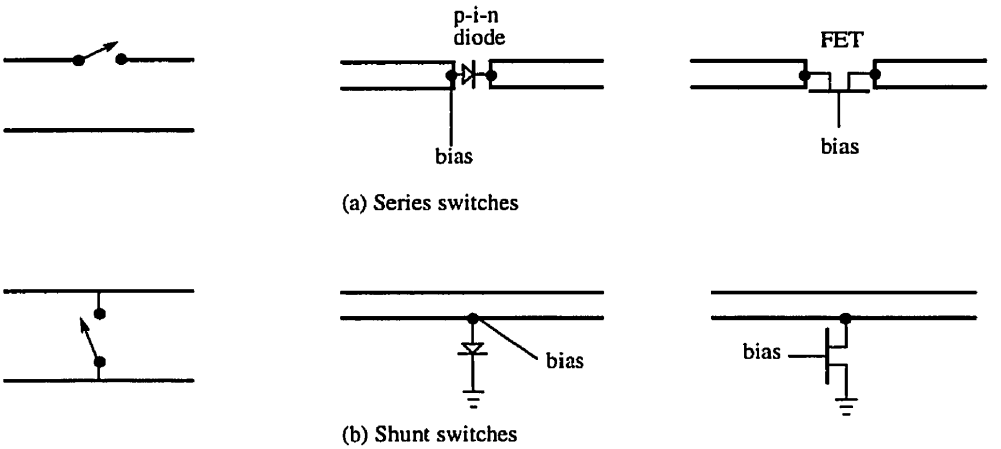


Figure 1.3 Semiconductor Device as Switches (a) series-mounted; (b) shunt-mounted

1.1.1 Switched-Line Phase-Shifter Circuit

Switched-line phase shifters are time delay circuits. Phase shift is achieved by passing the signal through different transmission line lengths. The phase delay $\Delta\phi$ between the two states is $\beta(l_1 - l_2)$, where $\beta = \frac{2\pi}{\lambda}$ is the propagation constant of the transmission line and l_1 and l_2 are the physical lengths. Figure 1.4(a) shows a series-mounted, and figure 1.4(b)

shows a shunt-mounted phase shifter circuit. In figure 1.4(b), when switches s_1 and s_1' are closed, the signal passes through the upper path. The input and output port see an infinite impedance through the lower path because the $\frac{\lambda}{4}$ sections are terminated with short circuits. A monolithic form of this circuit has been reported by Rogeaux et. al [ROGEAUX, 94].

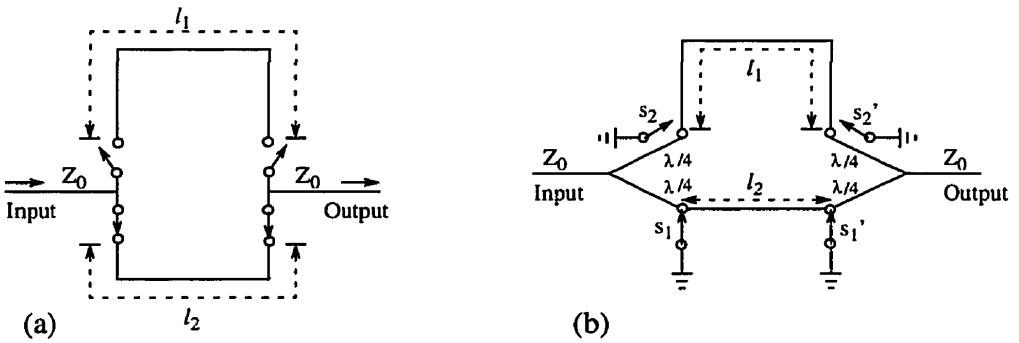


Figure 1.4 Switched Line Phase Shifter Circuit

1.1.2 Loaded-Line Phase Shifter

The loaded line phase shifter makes use of a transmission line loaded with a symmetric pair of switchable reactive elements [KOUL,91]. The reactive elements are separated by $\frac{\lambda}{4}$ so that the reflections from the reactive elements cancel at the input port at the designed frequency. Figure 1.5 shows a shunt-mounted loaded line phase shifter circuit.

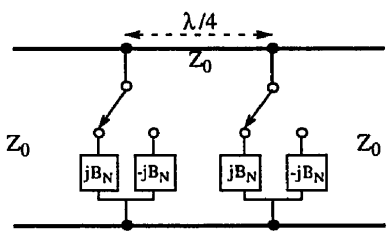


Figure 1.5 Loaded Line Phase Shifter Circuit

The phase delay between the two states is [GOYAL, 89]

$$\Delta\phi = 2\,\mathrm{atan}\left(\frac{B_N}{1-0.5B^2{}_N}\right) \tag{1.1}$$

This has been implemented in monolithic form byAyasli et al. [ANDRICOS, 85].

1.1.3 Reflection-type Phase Shifter

An example of a reflection-type phase shifter is shown in figure 1.6. Changing the state of the switch changes the reflection coefficient of the reflective network. This causes a change in phase delay between the two states. The phase difference $\Delta\phi$, for the specific case in figure 1.6 is equal to $2\pi\Delta l/\lambda$. The circulator routes the input signal to the reflective network and the reflection from the network is routed to the output port. For an ideal circulator, the transmission coefficient from the input to the output is equal to the reflection coefficient Γ of the reflective network. A monolithic implementation, which replaces the circulator with a 3 dB quadrature directional coupler, has been reported by [NAKAHARA, 93].

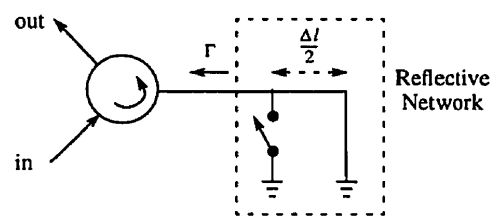


Figure 1.6 Circulator Coupled Phase Shifter

1.1.4 Switched High-Pass Low-Pass

The preceding phase shifters use transmission lines to realize reactive components. At lower frequencies (below 2GHz) the transmission lines become physically long. The switched high-pass low-pass technique shown in figure 1.7, uses lumped components to realize the filter. When the switches are connected to the high-pass section, the circuit

introduces a phase lead, and when the switches are connected to the low-pass section, the signal passing through the circuit undergoes a phase delay. Phase shift results from switching between the two filter circuits.

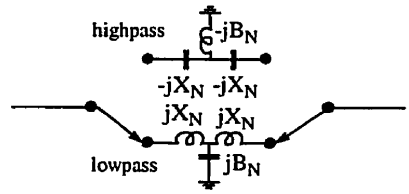


Figure 1.7 Switched High-Pass Low-Pass Phase Shifter

When the switches are connected as shown in figure 1.7. The transmission coefficient is given by [KOUL, 91]

$$S_{21} = \frac{2}{2(1 - B_N X_N) + j(B_N + 2X_N - B_N X^2_N)} \tag{1.2}$$

And the transmission phase ϕ_1 is given by

$$\phi_1 = \text{atan}\left[-\frac{B_N + 2X_N - B_N X^2_N}{2(1 - B_N X_N)}\right] \tag{1.3}$$

The transmission phase ϕ_2 when the switch is connected to the upper path is obtained by replacing B_N with $-B_N$ and X_N with $-X_N$ in equation (1.3). Therefore the differential phase shift is given by [KOUL,91]

$$\Delta\phi = \phi_1 - \phi_2 = 2\,\text{atan}\left[-\frac{B_N + 2X_N - B_N X^2_N}{2(1 - B_N X_N)}\right] \tag{1.4}$$

A FET switch implementation of the switched-filter circuit is shown in figure 1.8. When the control voltage V_1 is zero and V_2 is below the pinch off voltage V_p of the FET, the phase shifter is reduced to the circuit shown in figure 1.9. Where the "off" state FET

impedance is represented by a capacitor and the "on" state by a resistor. The circuit can be reduced further to the circuit shown in figure 1.10, if we assume that the "on" resistances are small compared to the impedance in parallel with them [GOYAL,89]. The circuit in figure 1.10 is a five section low-pass filter. For the case when V_2 is zero and V_1 is below the pinch-off voltage of the FET, the equivalent circuit is shown in figure 1.11. And can be reduced to the circuit as shown in figure 1.12, if r_3 and r_4 are small. If capacitors C_4 and C_5 have large impedances compared to L_2 and L_3, the circuit behaves like a fifth-order high pass filter.

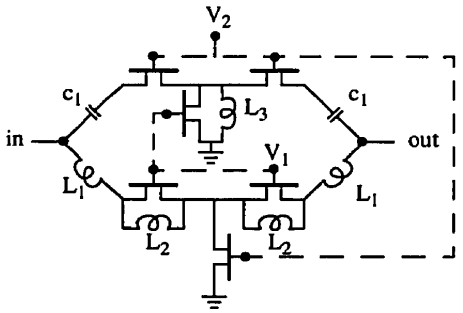


Figure 1.8 Switched High-Pass Low-Pass Phase Shifter using FET Switch

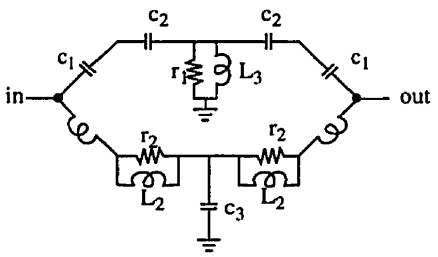


Figure 1.9 Equivalent Circuit of figure 1.8; for V_1=0 and $|V_2| > |V_p|$

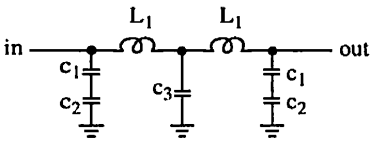


Figure 1.10 Simplified Circuit of figure 1.9

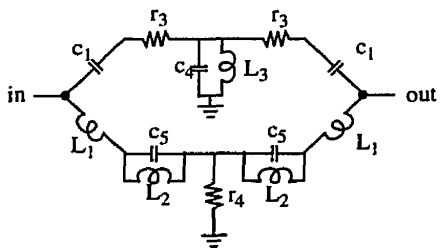


Figure 1.11 Equivalent Circuit of figure 1.8; for V_2=0 and $|V_1| > |V_p|$

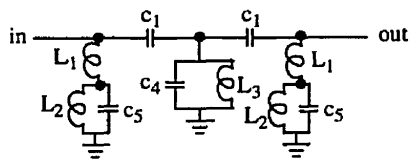


Figure 1.12 Simplified Circuit of figure 1.11

1.2 *Continuous Phase Shifter*

The preceding phase shifters use FETs as switches to realize the phase shift. We could also use the FET as a variable gain amplifier to realize a vector modulator. A block diagram is shown in figure 1.13. The 3dB, 90° coupler divides the signal into two equiamplitude quadrature signals. Then the signals are amplified by the dual-gate FET amplifiers, and the output of the FETs are summed in an in-phase combiner. The resulting vector sum at the output port is given by

$$C = A + jB = |C|e^{j\phi} \tag{1.5}$$

where $\phi = \text{atan}\frac{B}{A}$. The output phase ϕ can be controlled by changing the gain of the amplifiers. This method is also suitable for monolithic implementation.

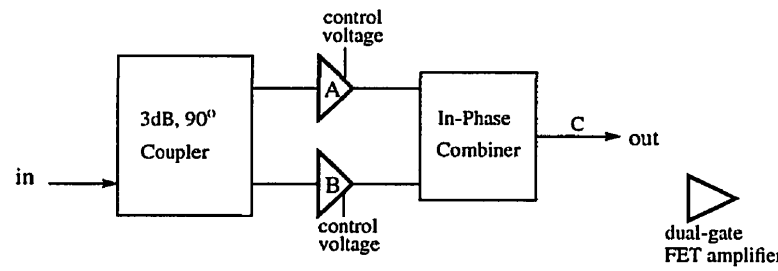


Figure 1.13 Vector Modulator Phase Shifter

The phase shifters that were discussed in the previous sections are applicable to microwave and millimeter-wave design. The circuits are commonly designed on a Gallium Arsenide (GaAs) substrate material. This is due to its semi-insulating properties and high electron mobility, allowing devices such as MESFETs to operate in the millimeter-wave range [ROBERSTON,95]. There has been a variable phase shifter reported which operates in the 100-160 MHz band [IMAI, 96], that uses silicon technology. However, the main interest of this thesis is on variable phase shifters for adaptive antenna applications which would operate in the 900MHz to 2.5GHz range. These are adaptive antennas that can be commercially used in the present wireless standards. Table 1.1 summarizes the spectrum allocations, multiple access method, channel spacing and other protocols that are applicable to digital cellular telephones. This thesis investigates the feasibility of using silicon bipolar homojunction transistor technology to realize a 1 GHz variable phase shifter.

1.3 Concluding Remarks

This chapter discusses different type of phase shifters including: switched line, loaded line, switched high-pass low-pass, and vector modulator techniques. Chapter 2 gives an introduction to adaptive antennas. Chapter 3 describes the circuits used to implement the programmable phase shifter. Chapter 4 shows the experimental measurements taken from the test chip.

Table 1.1Digital Cellular Standards

Standard	IS-54	IS-95	GSM
Mobile Frequency Range (MHz)	Rx:869-894 Tx: 824-849	Rx: 869-894 Tx: 824-849	Rx: 925-960 Tx: 880-915
Multiple Access Method	TDMA/FDM	CDMA/FDM	TDMA/FDM
Duplex Method	FDD	FDD	FDD
Number of Channels	832 (3users/channel)	20 (798 users/channel)	124 (124 users/channel)
Channel Spacing	30 KHz	1250 KHz	200 KHz
Modulation	pi/4 DQPSK	QPSK/OQPSK	GMSK (0.3 Gaussain Filter)
Channel Bit rate	48.6 kb/s	1.2288 Mb/s	270.833 kb/s

CHAPTER

Adaptive Antennas

2.1 Introduction

The demand for mobile communication units is increasing rapidly - in this age where information is the prime commodity. Therefore, the need for a bandwidth-efficient system is in order. Currently, Time Division Multiple Access (TDMA) and Code Division Multiple Access (CDMA) systems are being used to meet this need. In the research arena, numerous studies have been made [WINTERS,94; WU, 95; TSOULOS, 95] on the use of spatial diversity in conjunction with TDMA or CDMA to improve system capacity of wireless networks. Adaptive antennas can be used to spatially filter the desired mobile users, by forming radiation pattern nulls in the direction of the interfering signals (other mobile users), to allow a number of spatially-separate users to occupy the same frequency band. Winters et al. [WINTERS, 94] has demonstrated that for independent flat-Rayleigh fading wireless systems with N mutually-interfering users and with K+N antennas, N-1 interferers can be nulled out and K+1 path diversity improvement can be achieved by each of the N users. Another problem in mobile systems that could be addressed by spatial diversity is

the near-far effect. This refers to the reception of signals from geographically disparate sources. For example, a signal sent from a mobile unit near the base station would be received at a higher power level compared to the one that is sent from afar, since power loss is proportional to the fourth power of the distance. Agee [AGEE,94] showed that spatial and spectral diversity exploitation can allow separation of far more signals than conventional demodulation techniques at far greater disparities in received power level.

Adaptive antennas have been around since the invention of the single-sidelobe canceller by Howells [WIDROW, 85] in the late 1950's. Presently, there are numerous antenna array structures and algorithms that have been developed. However the advantage of adaptive antennas has not been exploited in commercial applications - though it has been used extensively in military applications - due to its computational complexity, which is constrained by technology and high cost. But recently, there have been significant advances in the field of adaptive signal processing and Very Large Scale Integration (VLSI) processing which would make this system viable for commercial use. This chapter presents some examples of structures, algorithms, and possible hardware implementations of adaptive antenna systems. However, since adaptive antenna constitute a broad field, we will concentrate on examples relevant to mobile communication systems.

2.2 *Classifications of Adaptive Antennas*

Adaptive arrays (we will use the words adaptive arrays and adaptive antennas interchangeably) is a broad field, with applications in seismic, SONAR, RADAR, and telecommunications signal processing. Therefore the word "Adaptive antenna" is ambiguous. A tentative classification is presented by [NICOLAU, 89]. They are classified according to:

1. The frequency operating bandwidth - narrowband or broadband. A bandwidth exceeding 5% deviation from the central frequency is usually accepted as a broadband criterion. An example of broadband signals are spread spectrum signals with a high spreading gain.

2. The types of signals being processed. They could be processed in the analog or digital domain. Our focus will mainly be on digitally processed signals.

3. The kind of information available. Adaptive antennas can deal with one of the following situations:

   - the desired signal to be received is unknown, but its direction of arrival (DOA) with respect to the array is known.
   - the desired signal to be received by the array is unknown, its DOA is unknown, but the desired power level is known.
   - the desired signal to be received by the array is unknown, its DOA is unknown, but the desired signal polarization is known.
   - no information about the desired signal is available at the receiver array, but as array operation progresses the processor "learns" to discriminate the desired signal from the undesired ones.

4. The performance measure to be optimized by the adaptation algorithm. The common performance criteria are: mean-square-error (MSE), signal-to-noise ratio (SNR), likelihood, noise variance, output power, and array gain.

5. The space in which the adaptation processes are taking place. The adaptation process can take place in time, frequency, and beams domain.

2.3 *Adaptive Linear Combiner*

Before we proceed with the discussion of adaptive antennas, it is helpful to look at the adaptive linear combiner to give us some insight about adaptive antennas. The structure of the linear combiner is generally applicable to most adaptive arrays. A diagram of the general form of adaptive linear combiner is shown in figure 2.1. The output of the system consists of the sum of the weighted inputs. The weight vector w_1, w_2,....., w_k, are adjusted according to some performance criteria. In the case where the desired response is known (statistically), the output of the linear combiner can be compared with the desired

response, and minimized in the mean-square-error sense. The analysis of this structure follows.

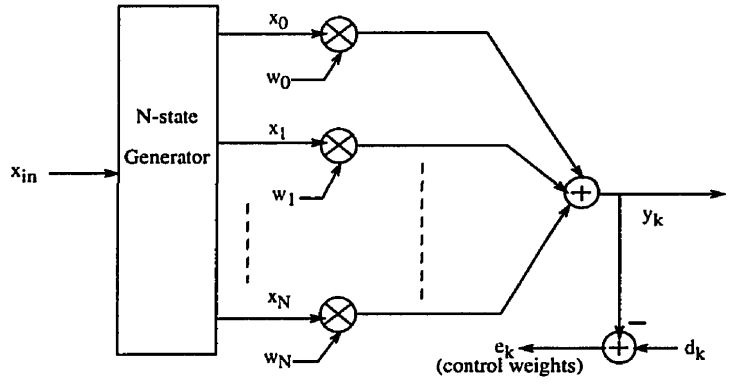


Figure 2.1 Adaptive Linear Combiner

First, we define the following:

$\mathbf{X_k} = [x_{0k}\ x_{1k}\ldots\ldots\ x_{Nk}]^T$ are the received signals sensed by the antenna array.

$\mathbf{W_k} = [w_{0k}\ w_{1k}\ldots\ldots w_{Nk}]^T$ corresponds to the weight vector which are adaptively adjusted.

y_k - is the output signal.

d_k - is the reference signal.

e_k - is the error signal.

The subscript k is used as a time index. From figure 2.1, the output signal y_k can be expressed as

$$y_k = \sum_{l=0}^{N} w_{lk} x_{lk} \tag{2.1}$$

or in vector notation

$$y_k = X_k^T W_k \tag{2.2}$$

From (2.2) we would like to find the optimum weight vector, $\mathbf{W}_{opt}$,that would make the output signal y_k match the desired signal d_k, one measure of this is the mean-square-error. Therefore we would like to minimize the mean-square-error (MSE) . To find $\mathbf{W}_{opt}$ in the minimum MSE sense, consider the error signal

$$e_k = d_k - y_k \tag{2.3}$$

Substituting (2.2) into (2.3), results to

$$e_k = d_k - X_k^T W = d_k - W^T X_k \tag{2.4}$$

The MSE can be written as

$$\xi = E[e_k^2] = E[d_k^2] + W^T E[X_k X_k^T] W - 2E[d_k X_k^T] W \tag{2.5}$$

Where E[x] is the expected value of x. Equivalently

$$\xi = E[d_k^2] + W^T R W - 2P^T W \tag{2.6}$$

where, $\mathbf{R}=E[\mathbf{X}_k\mathbf{X}_k^T]$ is the input correlation matrix, and

$\mathbf{P}=E[d_k\mathbf{X}_k]$ is the cross-correlation between the desired response and the inputs.

To find $\mathbf{W}_{opt}$ that would result to a minimum MSE, we take the gradient of $E[e_k^2]$ with respect to $\mathbf{W}$, which results in

$$\nabla = \frac{\partial \xi}{\partial W} = 2RW - 2P \tag{2.7}$$

and equate it to zero

$$2RW_{opt} - 2P = 0 \tag{2.8}$$

Equation (2.8) tells us that for a stationary input it is possible to find the optimum weight that would result to a minimum (MSE). This solution is usually referred to as the Weiner-Hopf equation for the adaptive linear combiner.

2.4 *Gradient-Based Algorithm*

In section 2.3, we found that the mean-square-error (MSE) ξ is a second-order function of the weight vector. The surface of the MSE in relation to the weight vector is a multi-dimensional paraboloid. The notion of having one minimum is inherent to this particular case and it applies to the N-dimensional space spanned by the weight vector. Our objective is to arrive at the optimum weight vector $\mathbf{W}_{opt}$ that would lead to the bottom point of the paraboloid. Gradient-based algorithms adjust the weight vector iteratively in accordance with an equation of the form

$$W_{k+1} = W_k + \mu(-\nabla_k) \tag{2.9}$$

where k is the iteration number, therefore $\mathbf{W}_k$ is the "present" weight value and $\mathbf{W}_{k+1}$ is the "new" value. ∇_k designates the gradient at the point $\mathbf{W}= \mathbf{W}_k$. The parameter μ is a constant that determines the stability and rate of convergence. The choice of μ is dependent on the eigenvalue spread of the input correlation matrix. *The entire family of gradient-based algorithms have only one purpose; to compute* ∇_k. The next section discusses two gradient-based algorithms. They are the steepest-descent and least-mean-square (LMS) algorithm.

We begin our discussion with the steepest-descent method. We found from (2.7) that

$$\nabla_k = 2(RW_k - P) \tag{2.10}$$

Substituting (2.10) into (2.9) results to

$$W_{k+1} = W_k + 2\mu(P - RW_k) \tag{2.11}$$

Equation (2.11) is the steepest-descent algorithm. It can be seen from (2.11) that the algorithm requires a knowledge of the desired response to compute the cross-correlation matrix **P**. A modification of the steepest-descent method is the least-mean-square (LMS) algorithm [WIDROW,85], where the instantaneous values for the correlation matrix $\hat{R}$ are used to estimate the gradient vector. This algorithm is computationally simpler than the method of steepest descent, because it does not require off-line gradient estimation or repetition of data [WIDROW, 85]. The derivation is as follows: we take the instantaneous value of the squared-error and take its gradient

$$\hat{\nabla}_k = \frac{\partial}{\partial W_k} e_k^2 = \frac{\partial}{\partial W_k}[d_k^2 + W_k^T X_k X_k^T W_k - 2d_k X_k^T W_k] \tag{2.12}$$

$$\hat{\nabla}_k = 2X_k X_k^T W_k - 2d_k X_k = 2X_k(X_k^T W_k - d_k) = -2e_k X_k \tag{2.13}$$

Substituting (2.13) into (2.9) gives us the LMS algorithm

$$W_{k+1} = W_k + 2\mu e_k X_k \tag{2.14}$$

The steepest-descent algorithm normally approaches the optimum values defined by the Weiner-Hopf equation, as the number of iterations approaches infinity. This is due to the exact measurements of the gradient vector. However, this is not the case for the LMS which relies on noisy estimate of the gradient vector. This causes the tap-weight vector of

the LMS algorithm to fluctuate around the optimum value as the number of iterations approaches infinity.

2.5 *Adaptive Antenna*

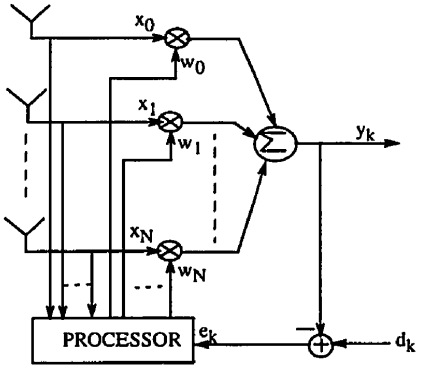


Figure 2.2 Adaptive Antenna

Figure 2.2 shows a common configuration of adaptive antennas. It is an adaptive linear combiner with the N-antenna elements generating the N-state vector. The error is formed between the difference between the output, y_k, and the reference signal, d_k. Using the error signal, the processor computes the weight values according to the performance measure chosen by the algorithm. For example, the steepest-descent algorithm would adjust the weight values in order to minimized the mean-square error. Other algorithms might adjust the weight values to maximize signal-to-noise ratio (SNR).

2.5.1 Single-Sidelobe Canceller (SSC)

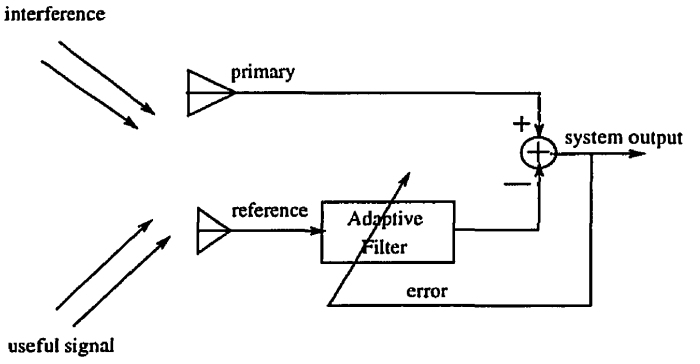


Figure 2.3 Adaptive Sidelobe Canceller

A simple form of adaptive antenna is the single-sidelobe canceller developed by Howells and Applebaum, shown in figure 2.3. Both the primary and reference antenna receive the useful signal plus interference. As shown in figure 2.4, the primary and reference input are related by

$$x_1(t) = x_0(t + \delta) \tag{2.15}$$

$$\delta = \frac{l \sin\theta}{c} \tag{2.16}$$

where c is the propagation speed of the planar wave, l is the length of separation between the two antenna, and θ is the direction of arrival. The sidelobe canceller can be seen as an adaptive linear combiner with d_k as the primary input, y_k as the reference input, and e_k as the system output, corresponding to the notation in figure 2.1. When the adaptive filter converges, the output of the filter will contain an interference component that matches the interference at the primary input. Therefore at the output, the interference cancels out, but the useful signal does not. The single sidelobe canceller can be extended to a multiple sidelobe canceller by adding reference antennas for every additional interferer. In general this type of structure can null N-1 interferers with N number of antennas. It is shown in

[WIDROW, 85] that this technique requires that the *interference signal be stronger than the receiver noise, and the information signal be weaker than the receiver noise.* The directivity pattern of the converged two-element sidelobe canceller is shown in figure 2.5, where the interferer's direction of arrival (DOA) is at $\theta = 60^{o}$ and l is λ (wavelength)/2.

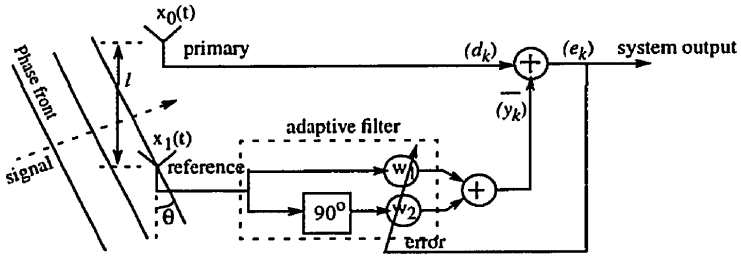


Figure 2.4 Adaptive sidelobe canceler seen as an adaptive linear combiner

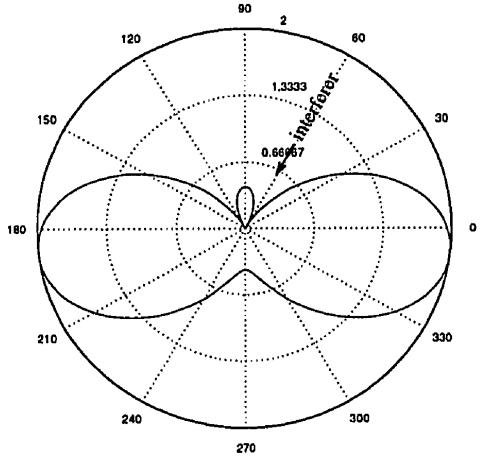


Figure 2.5 Directivity pattern of the converged two-element sidelobe canceler

The directivity pattern of a three-element sidelobe canceler is shown in figure 2.6. In this case two interferers from different direction but the same power is present at $\theta_1 = 25^{o}$ and

$\theta_2 = 60^o$. In both cases, the LMS algorithm is used to adjust the weights values and the receiver noises are ignored.

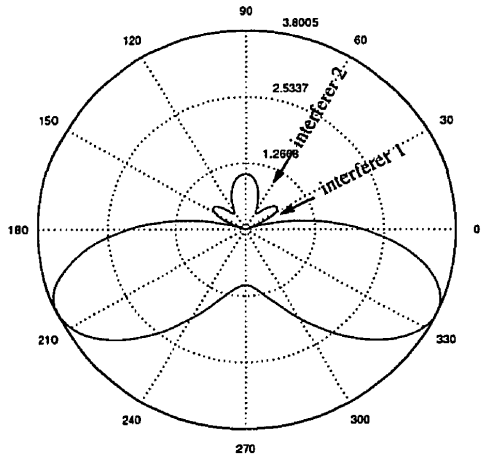


Figure 2.6 Directivity pattern of a converged three-element sidelobe canceler

2.6 Reference Signal Generation

The algorithms discussed in previous sections required the use of the desired response, obviously if we know the desired signal there's no need to transmit the information. However, the LMS algorithm doesn't need to know the desired response exactly. It only needs the desired response to be correlated with the signal and uncorrelated with noise and intereference. This makes the adaptive processing suitable for CDMA signals. Since the psuedorandom (PN) code in the signals are unique to each user and can be use in the generation of the desired response.

This section describes a reference signal generation technique for biphase modulated spread-spectrum signals. An example of a reference signal generation system is found in [COMPTON,88]. A biphase spread-spectrum signal can be represented by

$$y(t) = A_d e^{j[w_d t + \phi(t) + \psi_d]} \tag{2.17}$$

where A_d is the amplitude and w_d is the carrier frequency, ψ_d is the carrier phase, $\phi(t)$ is a binary waveform whose value switches between 0 and π. $\phi(t)$ is the modulo 2π sum of $\phi_{data}(t)$ and $\phi_{code}(t)$,

$$\phi(t) = [\phi_{data}(t) + \phi_{code}(t)] mod(2\pi) \tag{2.18}$$

where $\phi_{data}(t)$ is the information signal and $\phi_{code}(t)$ is the PN code sequence that is associated with each user, both waveform switch between 0 and π. The frequency f_c, of $\phi_{code}(t)$ is N times higher than that of $\phi_{data}(t)$. N is called the spreading ratio.

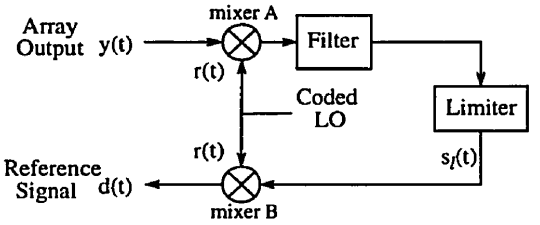


Figure 2.7 Reference Signal Generation Loop

The reference signal generation loop developed by Compton [COMPTON, 88] is shown in figure 2.7. The loop mixes the array output y(t) with a coded local oscillator, assuming that the PN code on the local oscillator is synchronized with the PN code on the array output. The waveform of the local oscillator r(t) has the form

$$r(t) = A_r e^{j[w_r t + \phi_{code}(t) + \psi_r]} \tag{2.19}$$

where A_r, w_r, and ψ_r are the amplitude, frequency and carrier phase angle of r(t). The sum product out of mixer A will be

$$y(t)r(t) = A_d A_r e^{j[(w_d + w_r)t + \phi_{data}(t) + 2\phi_{code}(t) + \psi_d + \psi_r]} \quad (2.20)$$

The term $2\phi_{code}(t)$ is always 0 or 2π since $\phi_{code}(t)$ switches only between 0 and π, so the product does not contain code modulation. Thus the output of the mixer only contains data modulation. Either product from mixer A may be selected by the filter. Mixer A's output is filtered, with the filter having enough bandwidth to pass the data modulation. The limiter only acts to the change the amplitude of the waveform to a constant value A_l. Afterwhich the signal is mixed again with r(t). If the sum product is chosen at mixer A, then the difference product is used at Mixer B, this gives

$$s_l(t)\hat{r}(t) = A_l A_r e^{j[w_d t + \phi_{data}(t) + \phi_{code}(t) + \psi_d + \psi_0]} = d(t) \quad (2.21)$$

Note that the desired signal frequency w_d becomes the reference signal frequency. and the presence of $\phi_{data}(t)$ and $\phi_{code}(t)$ makes the reference signal correlated with the desired signal. ψ_0 is the total phase shift in the loop, which must be adjusted to zero.

2.7 *Blind Adaptive Beamforming*

Blind adaptive beamforming stems from blind deconvolution techniques. Deconvolution refers to the problem of determining the impulse response (if the input signal is known) or input signal (if the impulse response is known) with the knowledge of the output signal. In the case of blind deconvolution, both the impulse response and the input signal is unknown (however statistical information about the input signal may be known).

2.7.1 Constant Modulus Algorithm

This section discusses a form of algorithm that doesn't require the use of an explicit reference signal. The constant modulus algorithm (CMA) exploits the constant envelope property of communication signals such as, frequency modulation (FM), phase-shift keying (PSK), and frequency-shift keying (FSK). The algorithm was first use by Godard for blind equalization in digital communication. The Godard algorithm minimizes the nonlinear cost function

$$\xi = E[(r_p(n) - |y(n)|^p)^2] \tag{2.22}$$

where

$$r_p(n) = \frac{E[|d(n)|^{2p}]}{E[|d(n)|^p]} \tag{2.23}$$

and p is a positive ingteger. Here d(n) and y(n) is the desired signal and the output signal (equation (2.2)) of the adaptive array, respectively. For the case where p=2, the algorithm is commonly known as the constant modulus algorithm (CMA). Similar to the LMS algorithm, the objective is to find the optimum weights that would minimize the cost function ξ. Recall from (2.9) that the weight vector is adjusted according to

$$W_{k+1} = W_k + \mu(-\nabla_k) \tag{2.24}$$

for this case [LITVA, 96]

$$\nabla_k = \nabla(E\{\xi(n)\}) = -E\{[r_p(n) - |y(n)|^2]y(n)x(n)\} \tag{2.25}$$

However, exact measurement of the gradient is not possible, since this requires a priori knowledge of $E[|d(n)|^p]$. However, we can make $|d(n)|$ equal to unity and use the instantaneous estimates; this results to

$$\nabla_k \approx -[1-|y(n)|^2]y(n)x(n) \tag{2.26}$$

Substituting (2.26) into (2.24) gives

$$W_{K+1} = W_k + \mu[1-|y(n)|^2]y(n)x(n) \tag{2.27}$$

From (2.27), we can see the similarity of the weight update equation for the LMS case, found in (2.14), where in this case

$$e_k = [1-|y(n)|^2]y(n) \tag{2.28}$$

Therefore, the same hardware configured for the LMS algorithm can be used for the constant modulus algorithm, except for the difference in the way the reference signal is generated. It should be noted that the CMA has a nonlinear cost function, which makes it nonconvex. This means that the algorithm might converge to a local minimum, and also the convergence of the algorithm is not guaranteed [LITVA,96].

2.7.2 Decision-Directed Algorithm

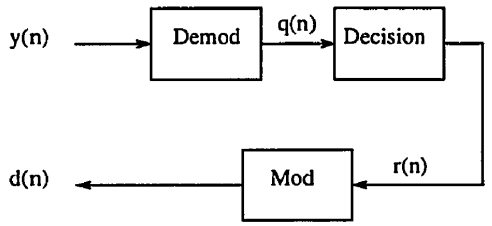


Figure 2.8 Reference signal generation for the decision-directed algorithm

The decision-directed algorithm makes use of past decisions as the reference signal. This is similar to the decision-feedback equalizer for the cancellation of inter-symbol interference (ISI). A conceptual block diagram of the reference generator is shown in figure 2.8. Decisions are made from the demodulated output signal, according to the known value of

alphabet that is closest to q(n). Afterwhich, the decision r(n) is modulated to be used as the reference signal. This algorithm has the disadvantage of suffering from error propagation if a wrong decision is made. The algorithm minimizes the cost function

$$\zeta = E[(d(n) - y(n))^2] \tag{2.29}$$

The same weight update equation in (2.24) can be used to find the optimum weight vector.

Both the CMA and decision-directed algorithm belongs to a class of blind deconvolution technique called the Bussgang algorithm, where the property of the Bussgang process,

$$E[y(n)y(n+k)] = E[y(n)g(y(n+k))] \tag{2.30}$$

is exploited for blind deconvolution [LITVA, 96]. In equation (2.30), g(y(n)) is some nonlinear function. In the case of CMA g(y(n)) = |y(n)|, and in the decision-directed algorithm , g(x) = decision(y(n)) = q(n).

2.8 *Programmable Phase Shifter*

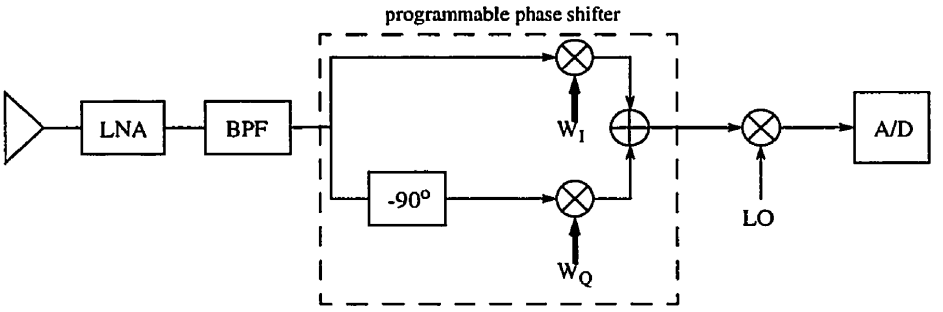


Figure 2.9 An Element of the Antenna Array Receiver

The thesis project is to build a programmable phase shifter which can be used in adaptive

antennas. Since the complex weighting of the signal is done in discrete steps, we would like to know the effects of weight quantization in the performance of the adaptive antenna. One possible configuration of a single element receiver of an adaptive array is shown in figure 2.9. The signal from the antenna element is amplified by a low-noise amplifier (LNA) and band-pass filtered (BPF) to eliminate out-of-band interference. The programmable phase shifter weights the signal according to the values determined by the adaptive algorithm. The weights w_I and w_Q are digitally controlled, through a digital word that comes from a digital signal processor. Then the signal is mixed with the local oscillator (LO) for downconversion to baseband. Afterwhich it goes through an analog-to-digital converter (ADC), so that the signal can be processed digitally. The same process can occur at an intermediate frequency (IF) as well.

We will use the single-sidelobe canceller (SSC) as an example. Shown in figure 2.10 is the directivity pattern of a converged array, where the inteferer's DOA is at $\theta = 60^o$. Also shown are the weight transients of w_1 and w_2 (notations are in reference to figure 2.4). In this case w_1 and w_2 can have any value as determined by the algorithm. However if we use discrete values of weights we find that the directivity pattern doesn't converge to the optimum value, this is shown in figure 2.11. The notch at $\theta = 60^o$ is 35dB higher than that in figure 2.10. In this example, the weights can only have values in discrete steps of $\frac{1}{2^5}$. It can be seen from figure 2.10 and 2.11, that the weight transients of the ideal and non-ideal case have similar transition pattern. The choice of μ is also of importance in the non-ideal case. For the ideal case, the small value of μ only causes the algorithm to converge at a slower rate. However, this is not the case when the weights have finite resolution. If μ becomes too small, it might not have a significant value to update the weight. The reason for this can be seen in (2.14), it says that the update algorithm depends on the error (e_k), input (x_k), and adaptation (μ) value, so if the their product is too small it won't update the

weight value. This is illustrated in figure 2.12, where the parameters used are the same as in figure 2.11, except the value of μ is 5 times smaller. It can be seen that the weight values doesn't come close to the optimal ones. And the weight pattern of w_2 doesn't have any transition.

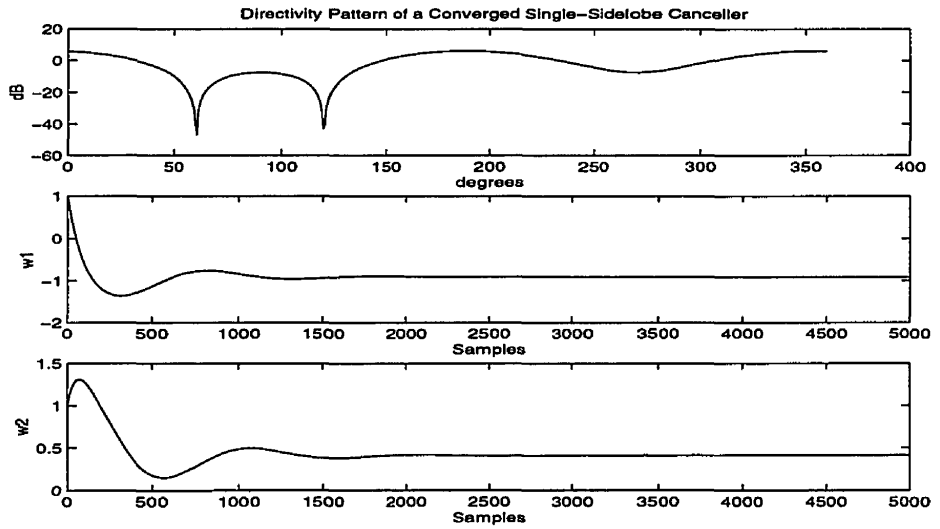


Figure 2.10 Directivity and Weight Pattern of the SSC with μ = 0.01

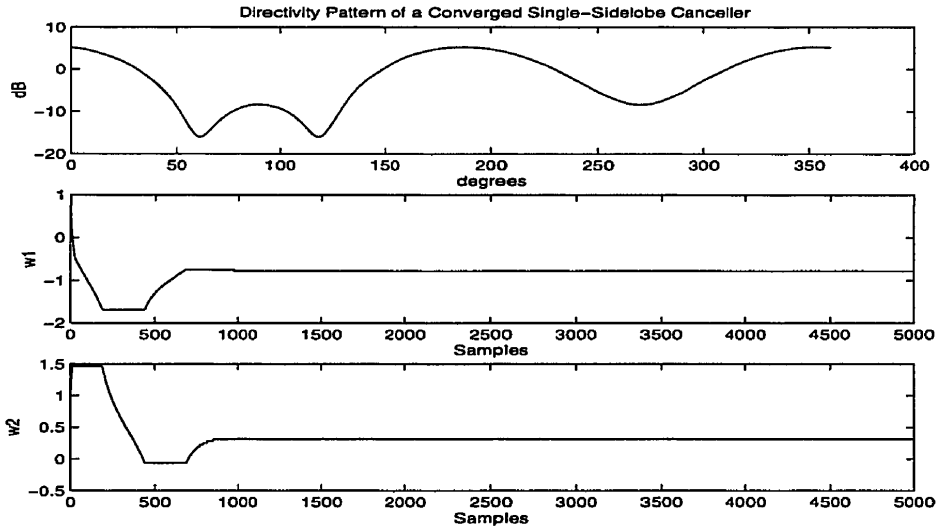


Figure 2.11 Directivity and Discrete Weight Pattern with $\mu = 0.05$ (step size=1/32)

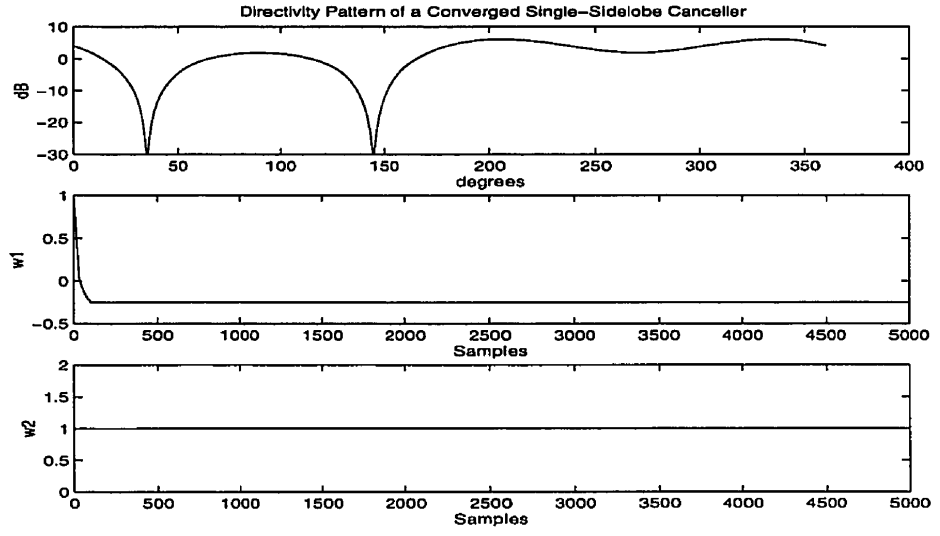
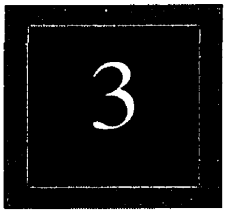


Figure 2.12 Directivity and Discrete Weight Patterns with $\mu = 0.01$ (step size=1/32)

CHAPTER

Circuit Implementation



3.1 Fundamental Principle

A variable phase shift can be achieved by a summation of two variable amplitude quadrature signals. This can be illustrated in a vector diagram shown in figure 3.1.

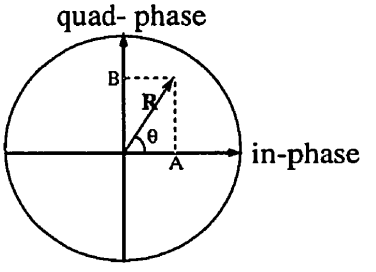


Figure 3.1 Vector Diagram

The resulting phase shift will depend on the relative amplitude of the quadrature signals. The phase shift can be made variable by controlling the amplitude of one or both of the quadrature signals. The vector **R** can be described in polar form as

$$R = \sqrt{A^2 + B^2} \angle \text{atan} \frac{B}{A} \tag{3.1}$$

One possible implementation of a tunable phase shifter is shown in figure 3.2.

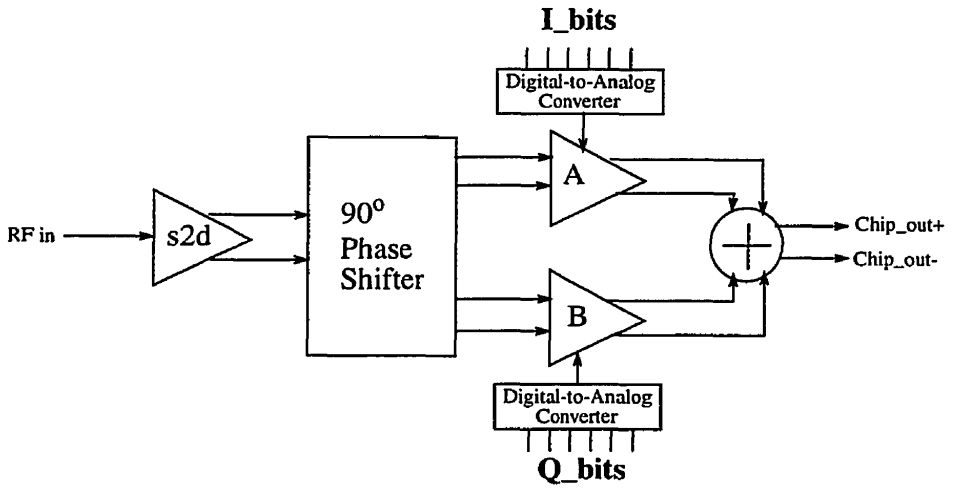


Figure 3.2 Block Diagram of Variable Phase Shifter

At the receiever end, we assume that the input signal comes from a single-ended low-noise amplifier. We would like to process the signal differentially in order to minimize second-order distortion and to double the signal-swing capability of the circuit for the same level of power supply voltage. Another advantage of having a fully-differential signal is that it minimizes the effects of interference from outside noise sources [PAUL, 92].Thus, the need for a single-to-differential converter (s2d). Then, the signal is split into two equi-amplitude quadrature signals by the 90° phase shifter. The quadrature signals are recombined, after each passes through a variable-gain amplifier, to form the phase-shifted output. Gain control of the variable-gain amplifier comes from a 6-bit current-mode digital-to-analog converter (DAC).

3.2 Circuit Description

3.2.1 Single-to-differential Converter (s2d)

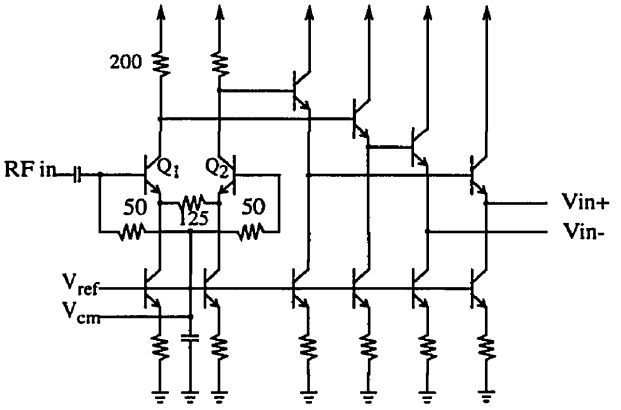


Figure 3.3 Single-to-Differential Converter

The input devices (Q_1 and Q_2) shown in figure 3.3 convert the single-ended signal into a differential signal. It also presents an input impedance of 50 ohm to the input source. It has a two-stage output buffer to supply the necessary current demanded by the next stage without loading the differential amplifier.

3.2.2 90 Degree Phase-Shifter

The 90° phase-shifter uses the RC polyphase network [GINGELL, 73] shown in figure 3.4. Its purpose is to split the signal into two differential equi-amplitude quadrature signals. This structure is preferred over the classic RC-CR filters, because its amplitude and phase to frequency characteristics are not as sensitive to the absolute values of R and C. Also, its amplitude deviation from the center frequency is minimal. The deviaton is less than 0.2 dB, within ±20 % of the center frequency. For example, if the center frequency is 1 GHz then the 0.2 dB bandwidth is 400 MHz. This makes the circuit suitable for broadband signals such as spread-spectrum. A plot of the frequency response of the circuit is shown in

figure 3.5. The phase plot shows a constant phase difference of 90 degrees between I_phase and Q_phase over a few of decades of frequency. The transfer function of the RC polyphase network is derived in Appendix A. Also shown in figure 3.6 is the group delay introduce by the network.

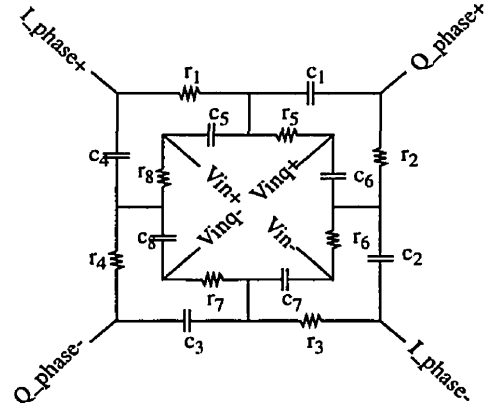


Figure 3.4 RC Polyphase Network

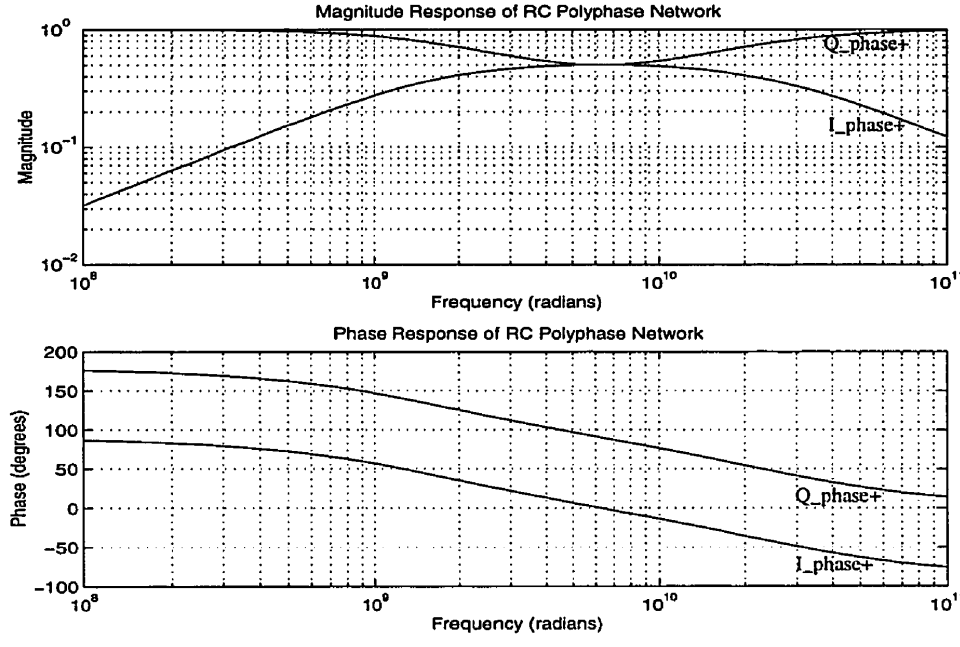


Figure 3.5 Frequency Response of RC Polyphase Network

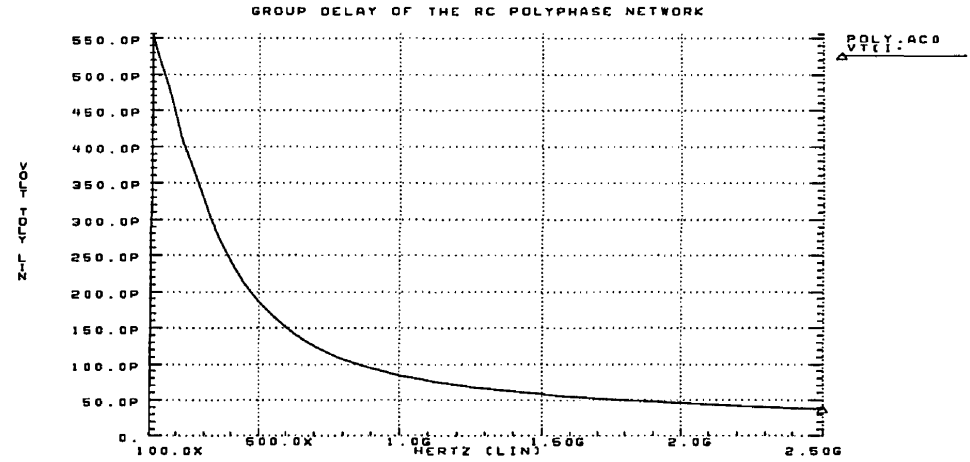


Figure 3.6 Group Delay of the RC Polyphase Network

Possible parasitic capacitance formed between the bottom plate of the capacitor and the substrate was simulated by introducing a capacitor between one side of each capacitor and ground. The value of the parasitic capacitance was chosen to be 20% of the desired capacitance. Figure 3.7 shows the magnitude response of the simulation. It shows a 10% change in amplitude level, however the center frequency is virtually unchanged.

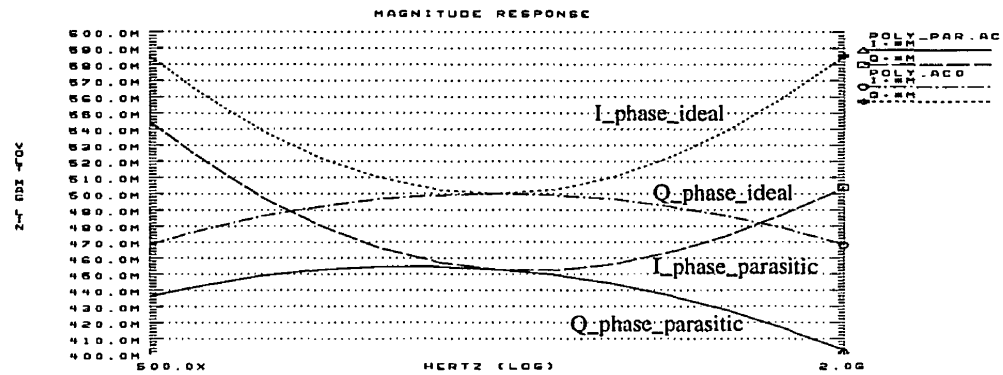


Figure 3.7 Magnitude Response of RC Network w/ Parasitic Capacitors

The phase difference between I_phase and Q_phase remains to be 90 degrees, although the absolute phase of I_phase and Q_phase are slightly shifted. The simulation result is shown in figure 3.8.

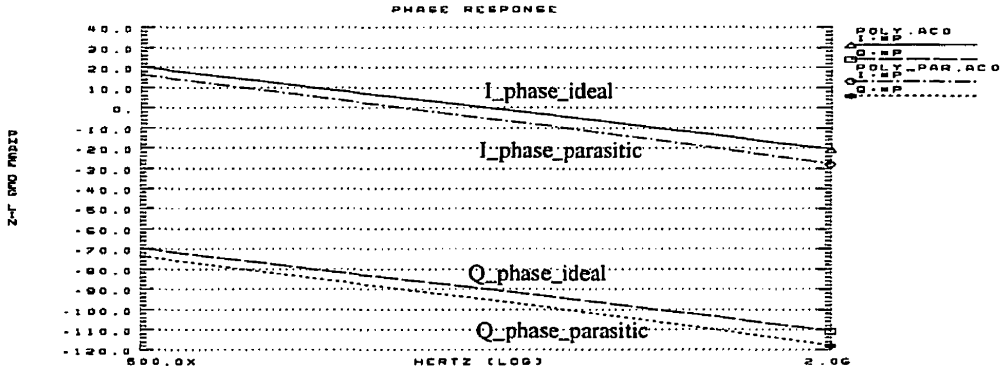


Figure 3.8 Phase Response of RC Network w/ Parasitic Capacitors

3.2.3 Variable Gain Amplifier

The variable gain amplifier is realized with a Gilbert multiplier shown in figure 3.9. The control current, Ictlp and Ictln, comes directly from a current-mode DAC, which will be discussed later. It can be shown that

$$Ioutp - Ioutn = 2i\frac{(Ictlp - Ictln)}{(Ictlp + Ictln)} \tag{3.2}$$

Equation (3.2) implies that in order to use this circuit as a variable gain amplifier we need to make the sum of Ictlp and Ictln be a constant, so that the gain of the amplifier is only proportional to the difference of Ictlp and Ictln. The current source Ib+i and Ib-i are the signal currents which comes from a transconductor. The transconductor is realized with a differential pair with emitter degeneration.

Since the output signal is in current form, the summation of the outputs from the two variable gain amplifiers is achieved by simply connecting the two output nodes together. The signals are then converted to voltage form by passing them through load resistors.

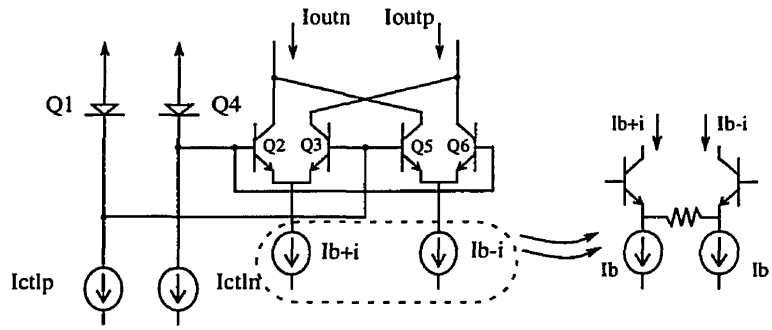


Figure 3.9 Gilbert Multiplier

3.2.3.1 Multiplier Dynamic Range

We now turn our attention to the dynamic range of the variable gain amplifier. Dynamic range is defined as the ratio of maximum-to-minimum signal amplitude that can be handled by the circuit. The minimum signal is limited by internally-generated noise and the maximum signal is limited by distortion. Distortion is an important consideration especially if this circuit is to be used for an adaptive antenna. It can severely distort the antenna beam pattern and thereby limiting the amount of interference cancellation achievable by an adaptive antenna system [XUE, 95].

To determine the noise sources of the multiplier, let us examine the emitter-driven variable gain amplifier shown in figure 3.10. At low attenuation, when V_{ctl} is low, the circuit behaves like a cascode amplifier with the output noise dominated by the noise sources of Q_1, R_E, and R_L. However, as the attenuation increases, with increasing V_{ctl}, the noise sources due to the base resistance of Q_3 and Q_4 start to dominate. The output noise peaks when Q_3 and Q_4 have equal collector currents. It is given by [SANSEN, 74]

$$v_{oN} = \sqrt{kT(r_{b3} + r_{b4})\Delta f}\frac{I_E R_L}{V_T} \quad V_{rms} \tag{3.3}$$

where Δf is the noise power bandwidth. Notice that the current I_E is directly proportional to the output noise of the circuit.

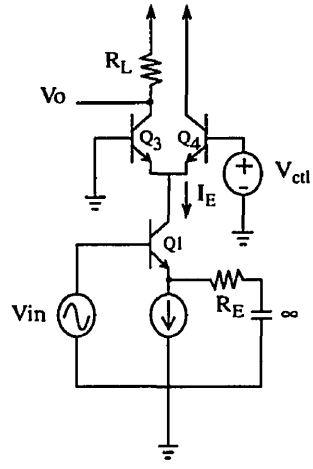


Figure 3.10 Emitter-driven Variable Gain Amplifier

In order to improve the distortion performance of the Gilbert multiplier, we need to have a highly-linear transconductor. This can be accomplished by increasing the current of the differential pair or by increasing the resistance of R_E. However, increasing R_E reduces the gain of the amplifier and increases the output noise of the circuit. Therefore choosing a higher current is a better option. At the same time, from equation (3.3) we would also need to reduce the noise contribution of r_{b3} and r_{b4} by reducing the currents in the quad transistors (Q_3 and Q_4). This leads us to the improved variable gain amplifier suggested by [SANSEN, 74], shown in figure 3.11. The resistor R_B provides the current which is the difference between I_p and I_E. Care must be taken, to ensure that the quad (Q_3,Q_4,Q_5, and Q_6)

and differential-pair (Q_1,Q_2) transistors are still operating near the optimum current required for high speed operation. The circuit in figure 3.11 was simulated in Hspice with and without R_B, at maximum gain. The improvement in dynamic range is shown in Table 3.1. Although R_B adds noise to the circuit, the addition of noise is offset by a reduction of the overall noise and improvement in linearity.

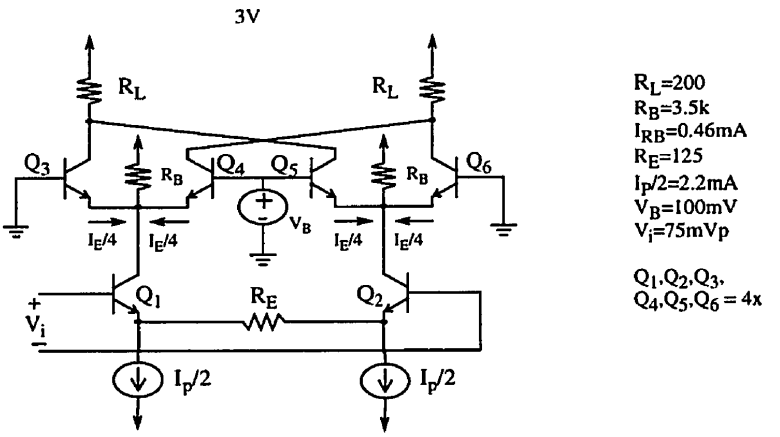


Figure 3.11 Gilbert Multiplier with Improved Dynamic Range

Table 3.1 Simulation Results of the Circuit in figure 3.11

	Without R_B	With R_B	% Improvement
Noise Figure (@ 1GHz) 50 ohm	17.2=12.4 dB	14.32=11.6 dB	16.7%
Total Harmonic Distortion	222m%	172m%	22.5%

The complete implementation of the two variable-gain-amplifiers with a summer is shown in figure 3.12

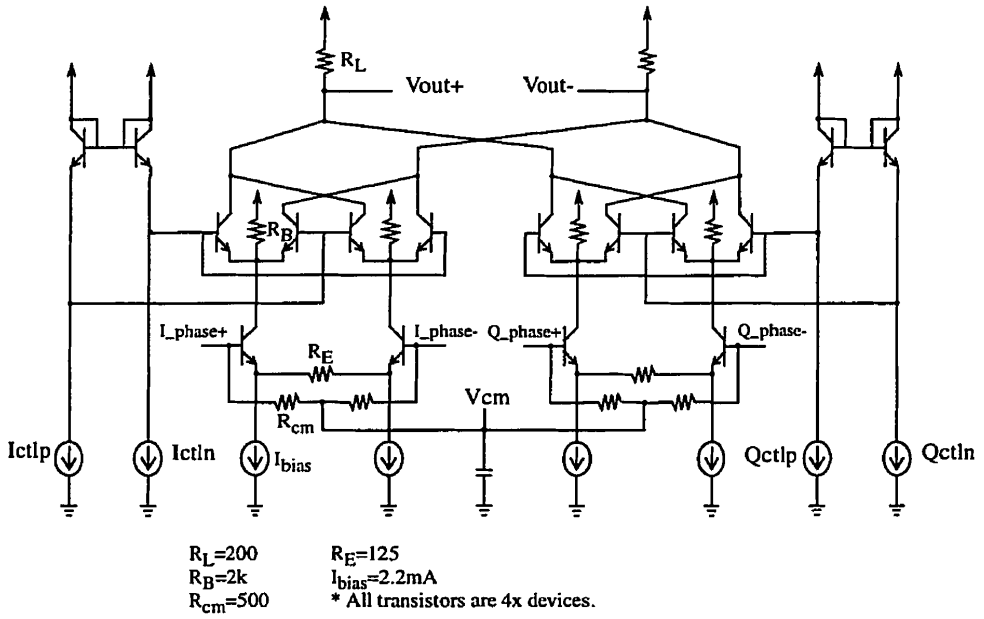


Figure 3.12 Variable Gain Amplifiers and Summer

3.2.4 Output Stage

The output stage consists of unity-gain buffers and a differential amplifier with a 50 ohm load, shown in figure 3.13. The differential amplifier output stage is preferred over an emitter-follower because the impedance looking into the emitter at high frequency is inductive. Therefore any significant capacitive loading on the circuit can cause instability.

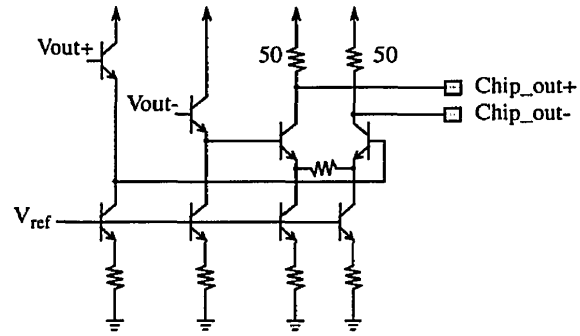


Figure 3.13 Output Stage

3.2.5 Digital-to-Analog Converter (DAC)

The DAC converter is segmented into a priority encoder [SCHEOFF, 79] and R-2R ladder converter, shown in figure 3.14.

3.2.5.1 Priority Encoder

The priority encoder ranks the switch (see figure 3.14) according to the significance of each bit. The "on" state of the more significant bit has a higher voltage level compared to the less significant bit, the voltage levels differ by 0.2V from one level to the next. For example, bout5 has a "high" level of 2.1 volts compared to 1.9 volts for bout4. The "low"

level are all the same at 1.5 volts. Table 3.2 summarizes the different logic (voltage) level for each bit, assuming a 3 volt power supply. Each level is separated by 200mV.

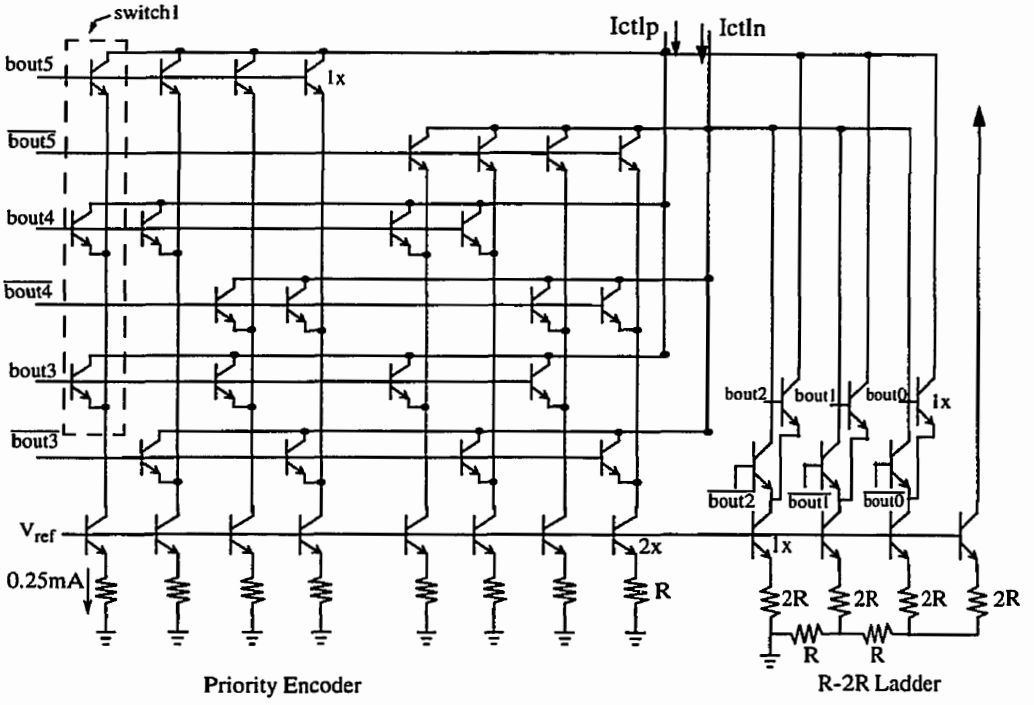


Figure 3.14 Segmented DAC

Each column of transistors in the three-bit priority encoder can be drawn as three transistors with their emitters connected together as shown in figure 3.15 (showing the first column as an example). Here, it can be seen that the current will steer toward the transistor with a higher base voltage. A voltage difference of 4 V_T (~ 100mV) is sufficient to switch the current to the transistor with a higher base voltage. Since the more significant bit has a higher voltage level, priority will be given to it when it is "high". The three less significant bits are realized using a current mode R-2R ladder. The currents are combined to control the gain of the variable gain amplifier. Notice that the *sum of Ictlp and Ictln* is always con-

stant, since the currents are only being steered from one node to the other. Thus, this can be used to control the variable gain amplifier as required by equation (1.2).

Table 3.2 Logic levels

Bit	Level(V)
bout5	2.1
bout4	1.9
bout3	1.7
low	1.5

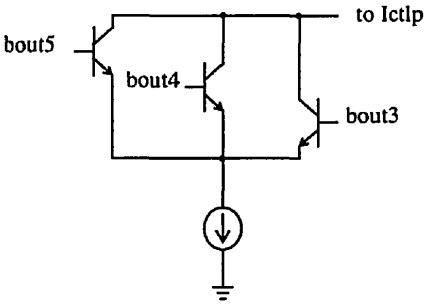


Figure 3.15 Circuit of a Column in the Priority Encoder

The multiple logic levels are achieved by the circuit shown in figure 3.16. The unity gain buffer Q_1 allows the input to operate between 0 to 3 volts. The two series diodes serve as reference level when the input goes low. This helps reduce the rise time from low to high, by preventing the current source Q_2 from entering saturation. Different "high" levels can

be achieved by using different values of R_{CM}. However, the sum of R_L and R_{CM} remains constant in order that the "low" level remains at 1.5V for all bits.

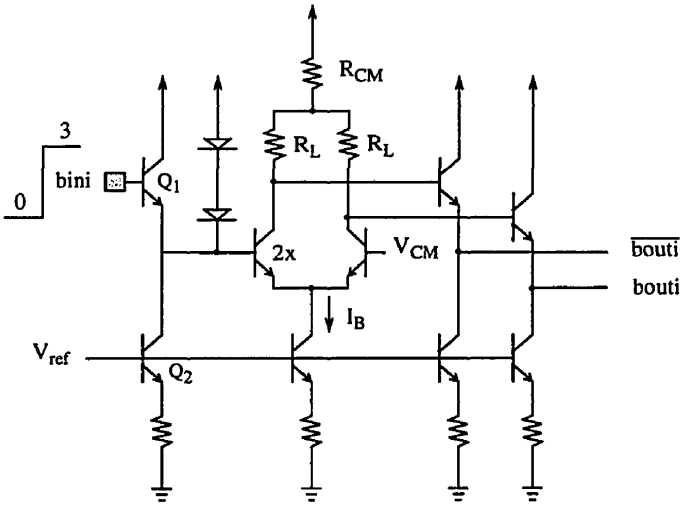


Figure 3.16 Multiple Logic Level Inverter

The output level is determined by the equation

$$bouti = Vcc - R_{CM}I_B - R_L I_B(bini) - V_{be} \tag{3.4}$$

where bini is logic "1" or "0".

3.2.5.2 R-2R Ladder

The popular binary-weighted R-2R ladder architecture is shown in figure 3.17. Q_1 and Q_2 are biased with current I_1. We solve for I_2 in terms of I_1 by following the loop around Q_2, 2R, R, 2R and Q_3, this gives

$$V_{BE2} + I_1 2R + 2I_1 R - I_2 2R - V_{BE3} = 0 \tag{3.5}$$

Therefore (for $V_{BE2}=V_{BE3}$; $A_4=2A_3=4A_2$)

$$I_2 = 2I_1 \tag{3.6}$$

Following the same procedure for the loop around Q_3, 2R, R, 2R, and Q_4, gives

$$V_{BE3} + I_2 2R + (I_2 + 2I_1)R - I_3 2R - V_{BE4} = 0 \tag{3.7}$$

which gives the relation

$$I_3 = 2I_2 = 4I_1 \tag{3.8}$$

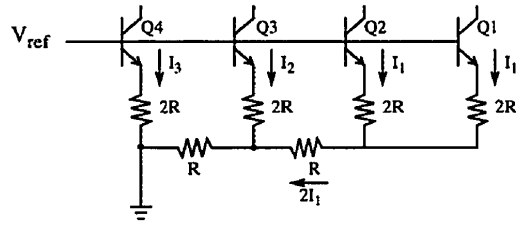


Figure 3.17 R-2R Ladder Network

Finally, note that the current sources of the priority encoder and R-2R ladder are in a cascode configuration after the currents are steered towards one side of the differential-pair-switch. Therefore the current sources have a high output impedance, which results in high compliance for the DAC.

3.2.6 Bandgap Voltage Reference

A bandgap voltage reference is used to set the voltage level of V_{ref}. The basic principle of a bandgap reference is to cancel the negative temperature dependence of a pn junction with a positive temperature dependence [MARTIN, 97]. Therefore V_{ref} can be written as

$$V_{ref} = V_{BE} + CT \tag{3.9}$$

where V_{BE} is the base-emitter voltage of a bipolar transistor, C is some constant and T is temperature in Kelvin. Expanding V_{BE} as a function of temperature and its collector current we have [MARTIN, 97]

$$V_{ref} = V_{G0} + \frac{T}{T_0}(V_{BE0} - V_{G0}) + (m-1)\frac{kT}{q}\ln\left(\frac{T_0}{T}\right) + CT \tag{3.10}$$

Where V_{G0} is the bandgap voltage of silicon at 0 Kelvin, k is the Boltzmann constant, m is a temperature constant, q is the magnitude of electronic charge, T_0 is the nominal operating temperature of the circuit, and V_{BE0} is the base-emitter voltage at temperature T_0. It can be shown that to cancel the temperature dependence of V_{ref} at the nominal temperature, we need C to be

$$C = \frac{V_{G0} + (m-1)\frac{kT_0}{q} - V_{BE0}}{T_0} \tag{3.11}$$

V_{G0} is approximately 1.204V and for T_0 =300°K and m=2.3, equation (3.11) results in

$$C = \frac{1.24 - V_{BE0}}{300} \tag{3.12}$$

The bandgap voltage reference used here is based on the circuit shown in figure 3.18 [GILBERT, 90]. Following the loop from Q_1, R_2, Q_4, R_1,Q_2, and Q_3, we have

$$R_1 I_4 + R_2 I_2 = V_{BE2} + V_{BE3} - V_{BE1} - V_{BE4} \tag{3.13}$$

for R_1=R_2

$$I_4 + I_2 = \frac{Vt}{R_1}\ln\left(\frac{A_1 A_4}{A_2 A_3}\right) = \frac{kT}{qR_1}\ln\left(\frac{A_1 A_4}{A_2 A_3}\right) \tag{3.14}$$

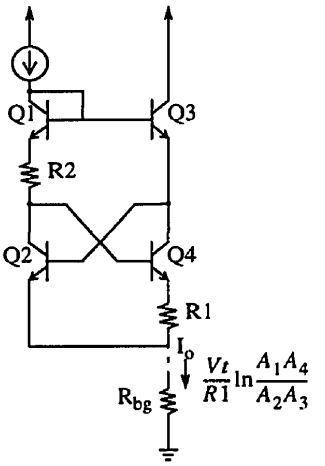


Figure 3.18 Generation of PTAT Current

Thus the current coming out of node I_0 is proportional to absolute temperature (PTAT). This configuration can be use as a simple bandgap reference, by placing a resistor at node I_0. The voltage at the base of Q_2 will be the bandgap reference and has the form V_{BE2}+CT, where

$$C = \frac{k}{qR_1}\ln\left(\frac{A_1A_4}{A_2A_3}\right)R_{bg} \tag{3.15}$$

Equation (3.15) satisfies (3.11) by choosing the right resistor value and transistor area. However, placing a load at the base of Q_2 could change the operation of the circuit due to the current drawn by V_{ref}. We have modified the circuit to the one shown in figure 3.19. We have for the circuit (assuming R_1=R_2)

$$V_{ref} = V_{BE1} + V_{BE4} - V_{BE5} + (R_1 + R_3)(I_2 + I_4) \tag{3.16}$$

Substitution of (3.14) into (3.16) results in

$$V_{ref} = V_{BE1} + \left[\ln\left(\frac{A_5}{A_4}\right) + \left(\frac{R_1 + R_3}{R_1}\right)\ln\left(\frac{A_1 A_4}{A_2 A_3}\right)\right]\frac{kT}{q} \tag{3.17}$$

where

$$C = \left[\ln\left(\frac{A_5}{A_4}\right) + \left(\frac{R_1 + R_3}{R_1}\right)\ln\left(\frac{A_1 A_4}{A_2 A_3}\right)\right]\frac{k}{q} \tag{3.18}$$

for the circuit in figure 3.19. Again (3.18) should satisfy (3.11). The circuit in figure 3.19 can supply the more current, compared to the circuit in figure 3.18, without severely affecting the level of the reference voltage.

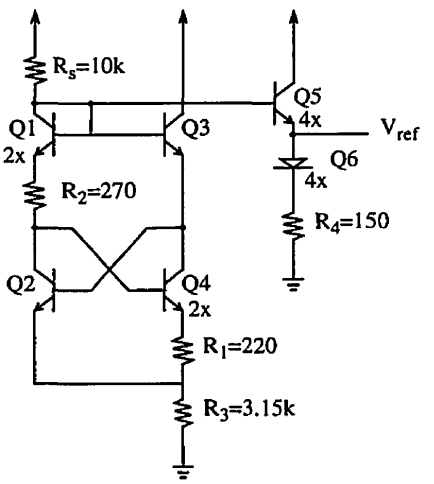


Figure 3.19 Bandgap Reference w/ more Current Driving Capability.

Finally, by slightly increasing the resistance of R_2, we could make V_{ref} substantially independent of power supply voltage. Figure 3.20 shows the simulation of the circuit in figure 3.19 vs. power supply voltage. The voltage reference is within ±1 % of the nominal 1.21 volts for a ±20% variation in supply voltage from the nominal 3.3 volts. The circuit

was also simulated with changes in temperature as shown in figure 3.21, it shows the typical bandgap temperature dependence with zero-temperature dependence at 30°C.

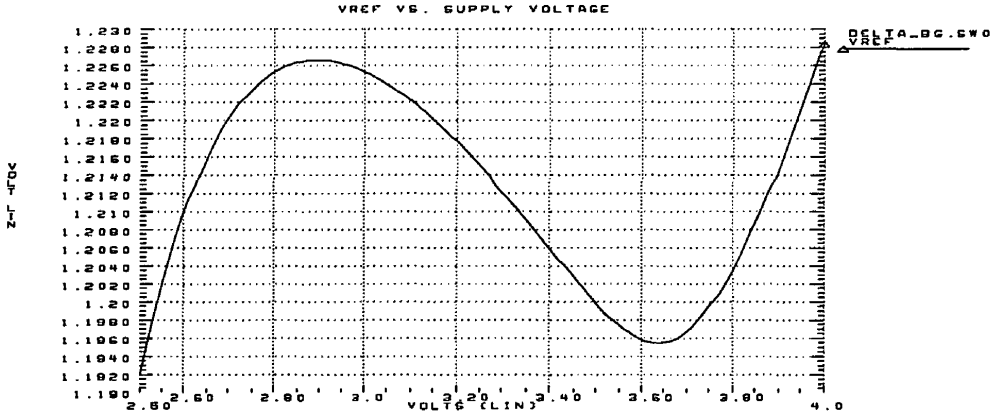


Figure 3.20 Vref vs. Supply Voltage

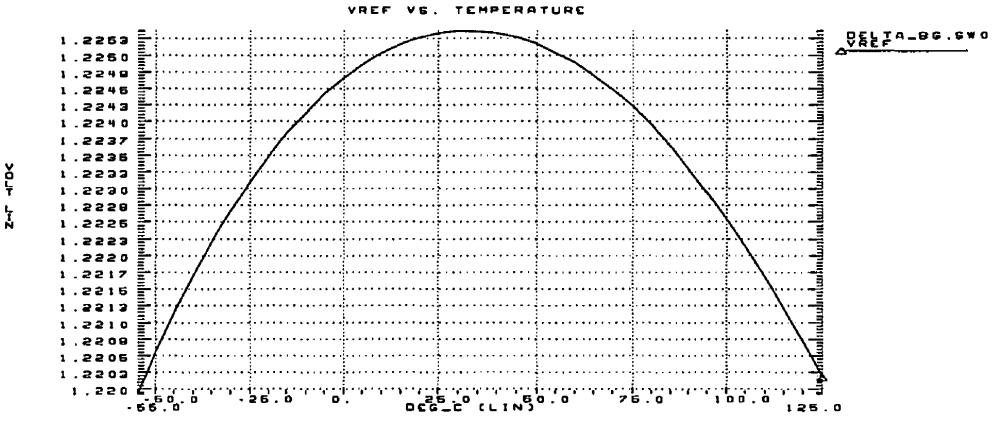


Figure 3.21 Vref vs. Temperature; Supply Voltage = 3 volts

3.2.7 Simulation of Programmable Phase Shifter

The various blocks are combined and simulated using HSPICE. Figure 3.23-21 shows the frequency response of the programmable phase shifter as the gain is kept constant, and the phase varied. This is done by changing the control word's (I_bits and Q_bits) logic level.

The control words are programmed to obtain vectors A, B, C and D in figure 3.22. The corresponding control bits are shown beside each vector. As expected, figure 3.23 shows that the magnitude of the ouput signals are the same for all four cases. While the phase of the output signals are 90° apart, relative to the adjacent test case, as shown in figure 3.24.

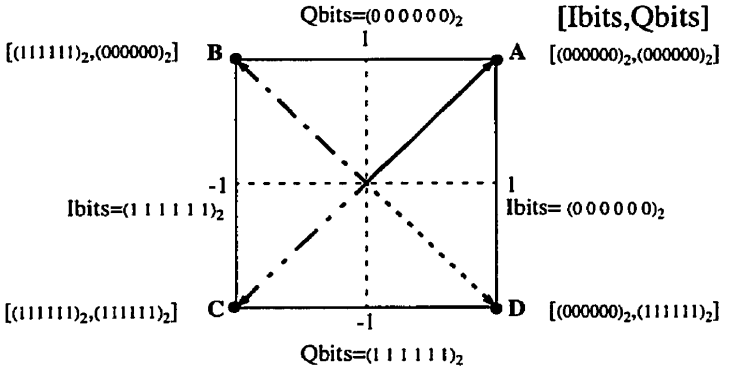


Figure 3.22 Test Cases for the Programmable Phase Shifter

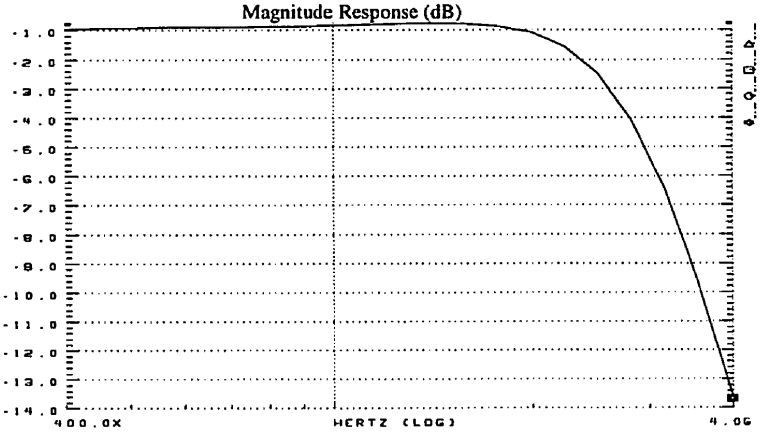


Figure 3.23 Magnitude Response for the Test Cases in figure 3.22

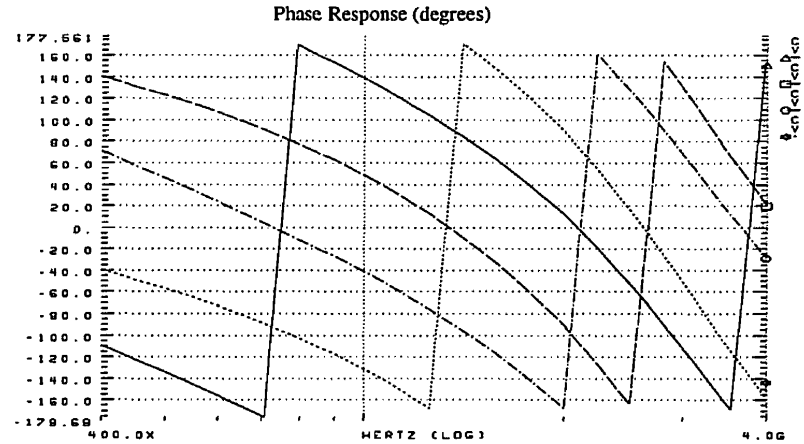


Figure 3.24 Phase Response of the Test Cases in figure 3.22

Figure 3.25 shows the transient response of the circuit to a 1GHz sinusoid for all test cases in figure 3.22.

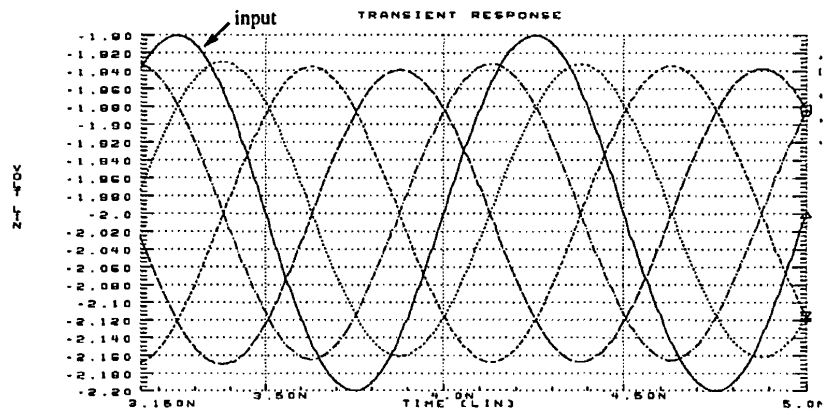


Figure 3.25 Simulated Transient Response of the Circuit to a 1 GHz sinusoid

Layout of the circuit was done in Mentor GDT using the Ballistic interface. The chip area is 1.36x1.46 mm^2. This small size allows for 16 channels to be included in a single chip

with a maximum of 8 mm on a side, which is a very reasonably sized chip. The digital-to-analog converters have their own bias circuits, which are separated from the circuit blocks that operate at high frequency. On-chip decoupling capacitors were placed on vacant silicon areas. The power and ground connections were each made through four bondpads to lower ground resistance. The high frequency input and output signal bondpads were placed near Vcc and Vss bondpads, to reduce radiated emission loop area on the printed cirucit board. The circuit layout is shown in figure 3.26.

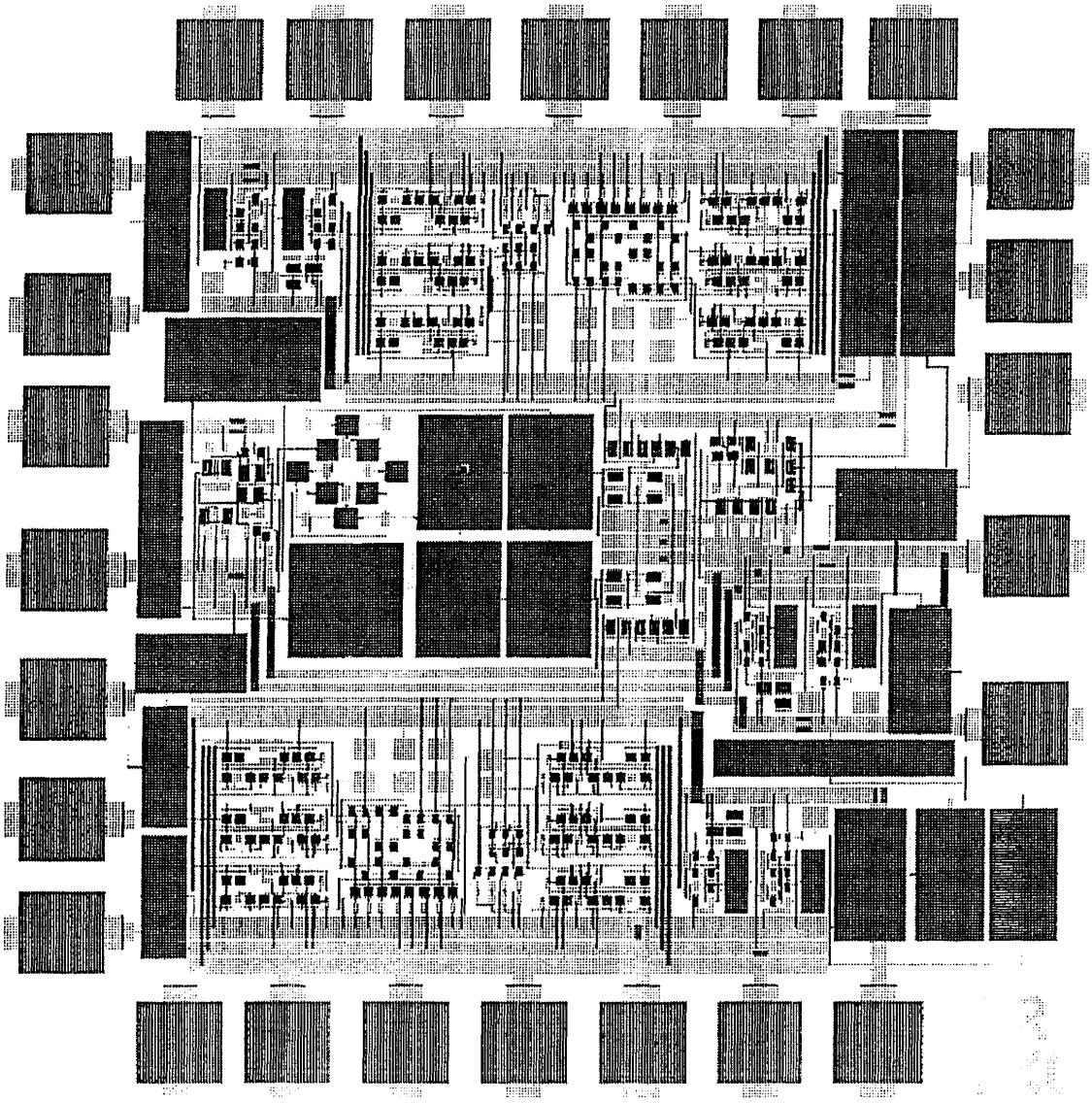
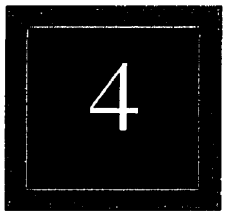


Figure 3.26 Layout of the Circuit

CHAPTER

Testing



This chapter discusses the testing results from measurements performed on the circuit.

4.1 Test Board

The test board used was provided by Canadian Microelectronics Corporation (CMC). The test board is designed for the (Bell-Northern Research) BNR 28/44 CQFP (Ceramic Quad Flat Pack) package, which is also available through CMC. Both the package and test board are designed to handle signals with frequencies up to 1.5 GHz. The test board is characterized using time-domain reflectometry (TDR) techniques in order to account for the measurement effects introduced by it to the chip. The test board connects to the external test environment through SMA connectors. The signal paths from the package to the SMA connectors are through 50-ohm controlled-impedance lines (a microstrip implementation) [CMC, 96]. The layout of the test board is shown in figure 4.1. The inputs are at U42 and U28, and the differential outputs are taken at U34 and U35.

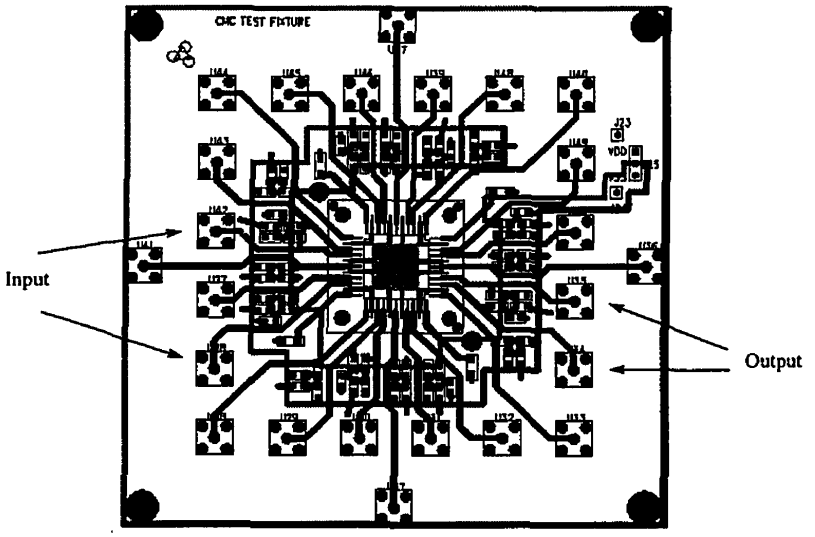


Figure 4.1 Layout of Printed Circuit Board Test Fixture

4.1.1 Time-Domain Reflectometry(TDR)

Time-domain reflectometry was used to measure the equivalent line impedance of the test board. This was done by sending a RF pulse into the transmission line so that if the wave encounters a change in line impedance, part of it will be reflected. The TDR test setup for the PCB-TF is shown in figure 4.2. The return time and shape of the reflected wave can be measured from which information about the characteristic impedance of the transmission line is determined. The reflection coefficient at a load Z_L in a transmission line with characteristic impedance Z_0 is

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{4.1}$$

where V_{refl} and V_{inc} are the incident and reflected voltages, respectively. For example, if a step voltage of amplitude V_p is launched at one end of the transmission line and takes $\frac{T}{2}$ seconds to reach the load, the reflected voltage V_{refl} is returned to the input with a T second delay. V_{refl} will then be added to the original step function. The resulting waveform after time T will depend on the characteristic impedance of the load. Figure 4.3 illustrates the voltage waveform seen at the generator after a step function with amplitude V_p is launched. Figure 4.3(a) shows the voltage waveform for an open circuit load and figure 4.3(b) shows for a short circuit load.

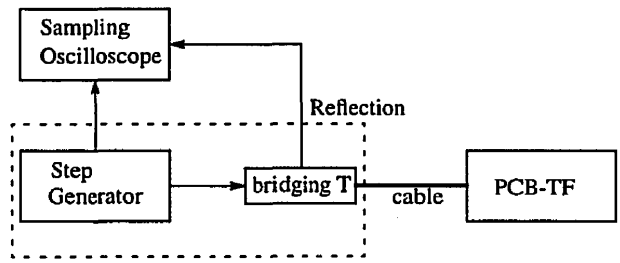


Figure 4.2 TDR Test Setup for the PCB-TF

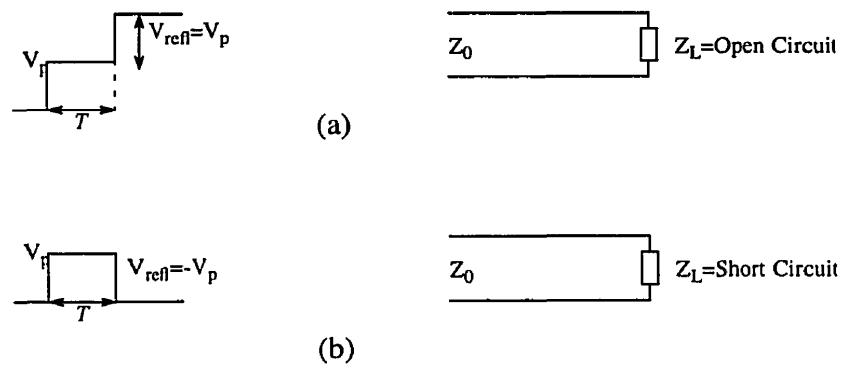


Figure 4.3 Characteristic Responses to Time Step Functions

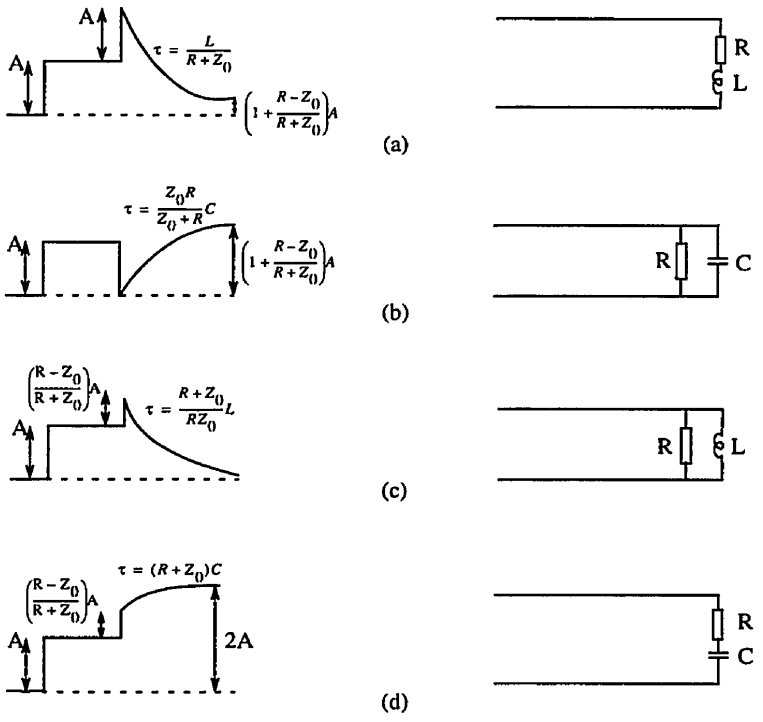


Figure 4.4 Responses to RC and RL Load Impedance

Figure 4.4 shows the response for different RC and RL load impedances. These figures can be compared with the measured results and then used to determine the approximate component values at the load. We can predict the waveforms in figure 4.4 intuitively. For example, in the case of figure 4.4(a), the inductor looks like an open circuit at high frequency (which comprise the initial step), so we would expect an open-circuit type response initially. Then at low frequency it looks like a short, so as the step input settles only the resistance R is seen by the generator. In between the initial and final value is the typical exponential decay. For an exponential response, it takes 0.69τ to reach half the final value from the initial value. Since τ, Z_0, and the step amplitude (A) are known or can

be measured, we can calculate the equivalent lumped components seen by the generator. Figure 4.5 shows TDR measurements for the following: a) cable only, b) cable connected to U34, and c) cable connected to U35. All of them have open-circuit terminations. The notch at time ~ 20.9ns for (b) and (c) waveform is caused by the SMA connectors. We can compute the approximate impedance introduced by the connectors by comparing it to the known waveforms shown in figure 4.4. Figure 4.4(b) is a good match. From figure 4.5, 0.69τ was measured to be 40ps. Z_0 and A are known to be 50 ohm and 0.2 volts respectively. Using the equations in figure 4.4(b) , the equivalent impedance seen by the source is shown in figure 4.6.

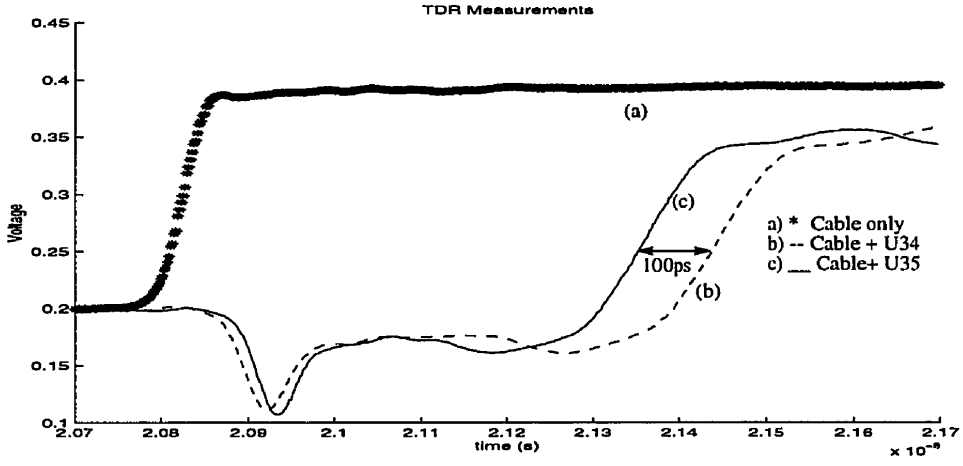


Figure 4.5 TDR Measurement

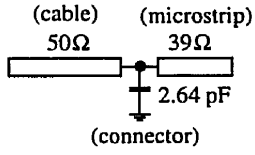


Figure 4.6 Equivalent Impedance of Cable to Microstrip Transition

Figure 4.6 shows that the board can only handle signals with frequencies up to 1.5GHz, since the RC(microstrip-to-connector) time constant has an approximate cutoff frequency of 1.5GHz.

Time-domain reflectormetry is also used to determine the difference in electrical length between two signal paths. We need to take this into account since we are measuring differential signals. Figure 4.5(b) and (c) shows the difference in time delay between two output path: U34 and U35. It shows that it would take 50ps (one way=100ps/2) more time for the signal to travel along U34 relative to U35. This is equivalent to an 18^{o} phase shift at 1 GHz.

4.2 *Bias Stage*

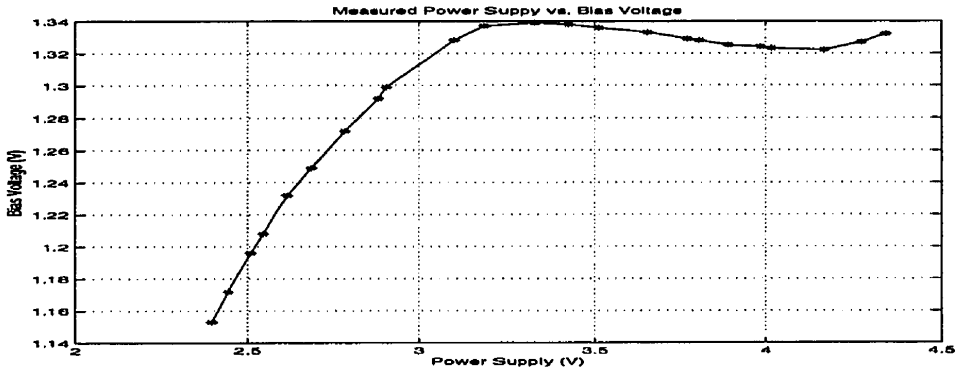


Figure 4.7 Power Supply vs. Bias Voltage

The bias circuit was measured with respect to changes in the power supply voltage. As shown in figure 4.7, a 50% increase in supply voltage (from 2.8 to 4.3), causes a 3% increase (from 1.3 to 1.34) in bias voltage. The bias voltage deviated from the bandgap voltage due to the variance of the control resistor.

4.3 Programmable Phase Shifter

The test set-up for measuring the time response is shown in figure 4.8. The chip is mounted on the printed circuit board shown in figure 4.1. The signal generator provides a 1GHz signal at a level of -3dBm. This is displayed on the oscilloscope as a 418mVpp sinusoidal signal, instead of the expected 447mVpp, due to minor impedance mismatch from the generator to the oscilloscope. To illustrate the functionality of the circuit, the control bits are changed in order to obtain vectors A, B, C and D in figure 4.9. The corresponding control bits are also shown beside each vector. Figure 4.10 shows the output of the circuit as displayed on the oscilloscope for all four cases. The phase difference of the vectors relative to their neighbors is expected to be 90°. The phase response of the experimental results matched the expected results. The maximum error is 8° for this case. The 10% deviation arises from errors in amplitude ratio between amplifier A and B. The amplitude errors in turn comes from errors in current ratio between the two DAC.

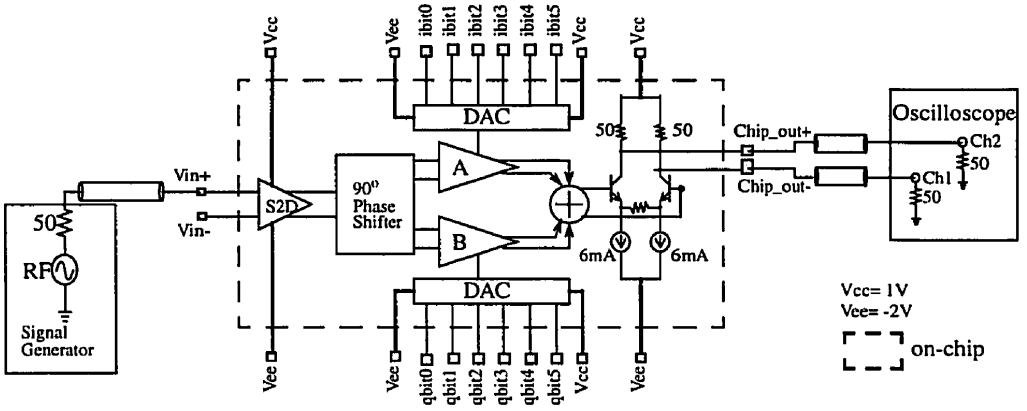


Figure 4.8 Test Set-up for the Time Response

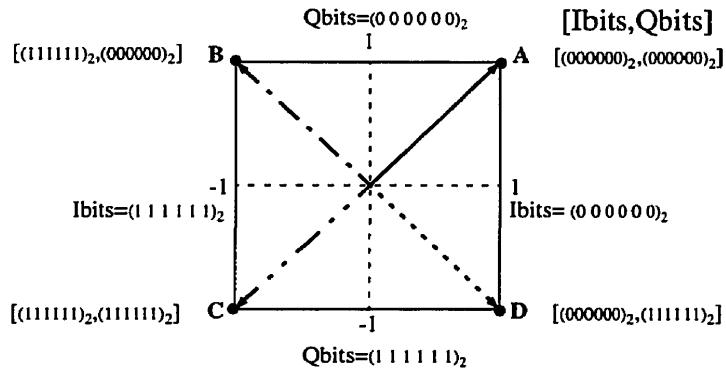


Figure 4.9 Test Vectors

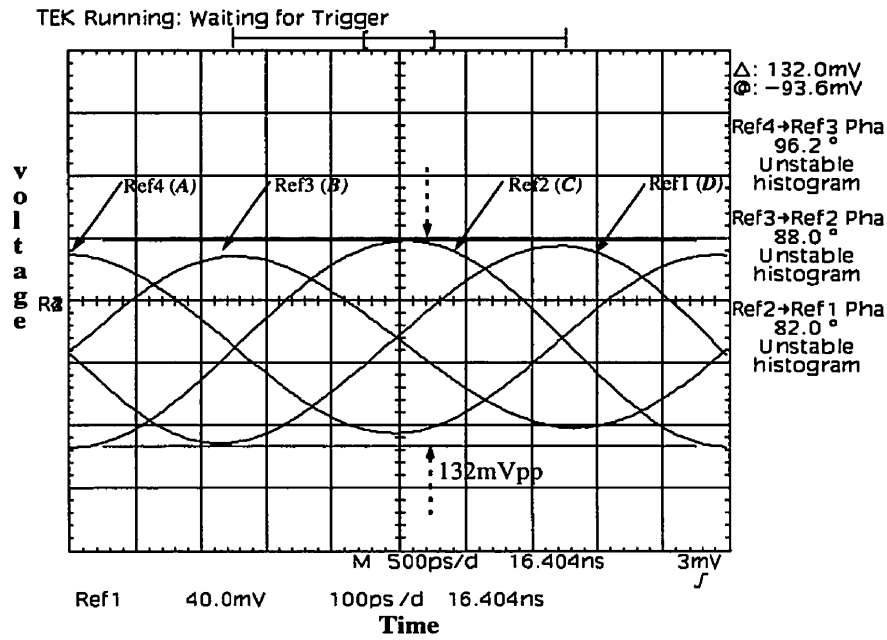


Figure 4.10 Oscilloscope Display

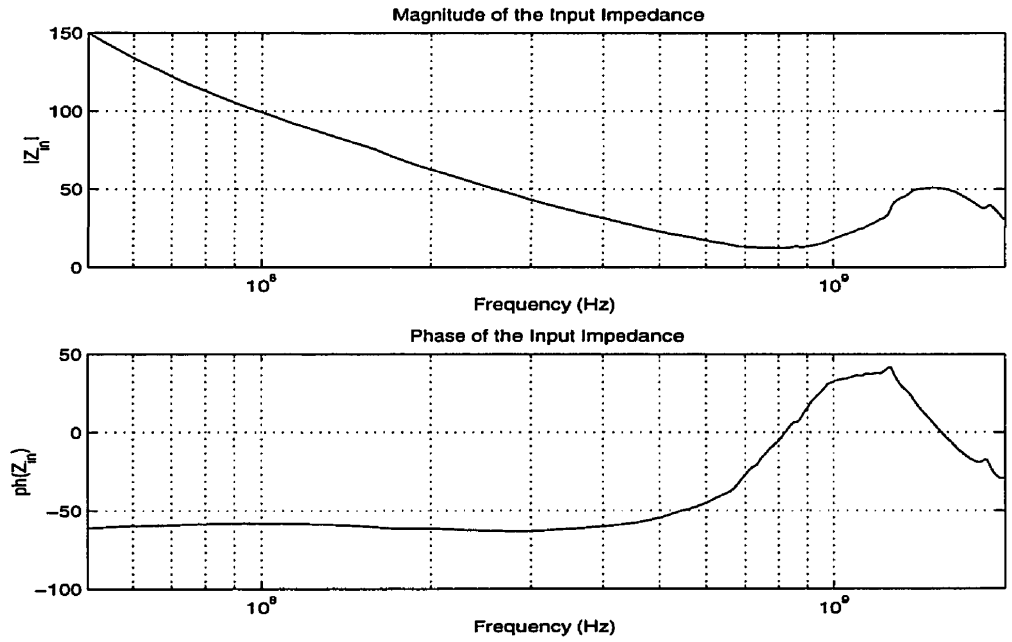


Figure 4.11 Input Impedance vs. Frequency

Simulation of the test set-up (figure 4.8) predicts a power gain of -0.7 dB for a 50 ohm load. However, experimental result shows a gain of -10 dB (20log[132/418]). The decrease in power gain is attributed to the impedance mismatch caused by the package and the board, which was not modelled in simulation. Shown in figure 4.11 is the input impedance measured at the SMA connectors, versus frequency. The output impdeance was also measured and its frequency response exhibits similar characteristics at 1 GHz. From figure 4.11, the magnitude of the input reflection coefficient (S_{11}), assuming a 50 ohm load, at 1 GHz was computed to be 0.55, which means that the maximum power that can be transferred to a matched load, from the generator, has already been reduced by 5 dB (20log[0.55]) at the connectors. This applies to the output connectors as well.

The transmission coefficient (S_{21}) of the programmable phase shifter is also measured with a vector network analyzer. The S_{21} from the two output ports were measured separately and the data points were recorded. Since they are differential signals, their difference was computed in Matlab. The 50ps time delay between the two trace length was also taken into account. The control bits: qbit0, qbit1, qbit2, qbit3, qbit4 and qbit5, are turned "on" alternately, with ibit3 also "on" for all cases. Figure 4.12 shows the phase response and the power gain ($|S_{21}|^2$) of the circuit. It is evident from figure 4.12 that the digital-to-analog converter is functioning, since the change in gain and phase is proportional to the significance of the bit. The more significant bit introduces more attenuation and phase shift.

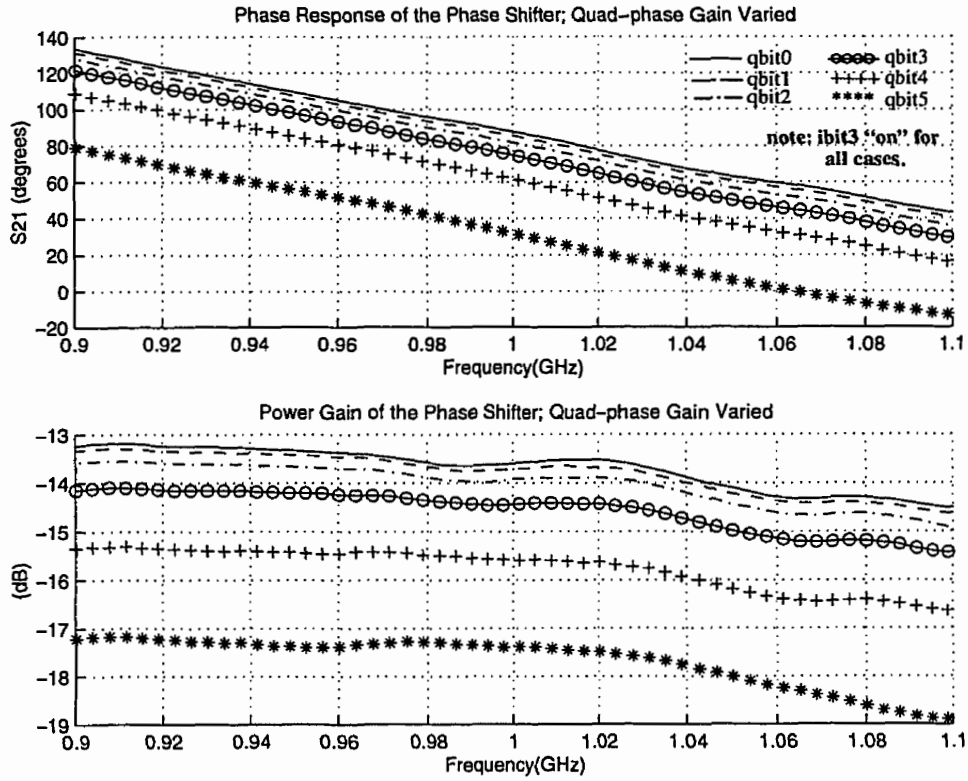


Figure 4.12 Frequency Response of Phase Shifter as the Quadrature gain is varied

The harmonic distortion is determined by taking the fast fourier transform (FFT) of the waveform in figure 4.10. The built-in FFT function of the Tektronix TDS 820 oscilloscope was used to resolve the frequency components of the signal. The signal is windowed with a Hamming window. The result of the FFT is shown in figure 4.13. Table 4.1 shows a summary of distortion measurements for the 1 GHz test signal. Th

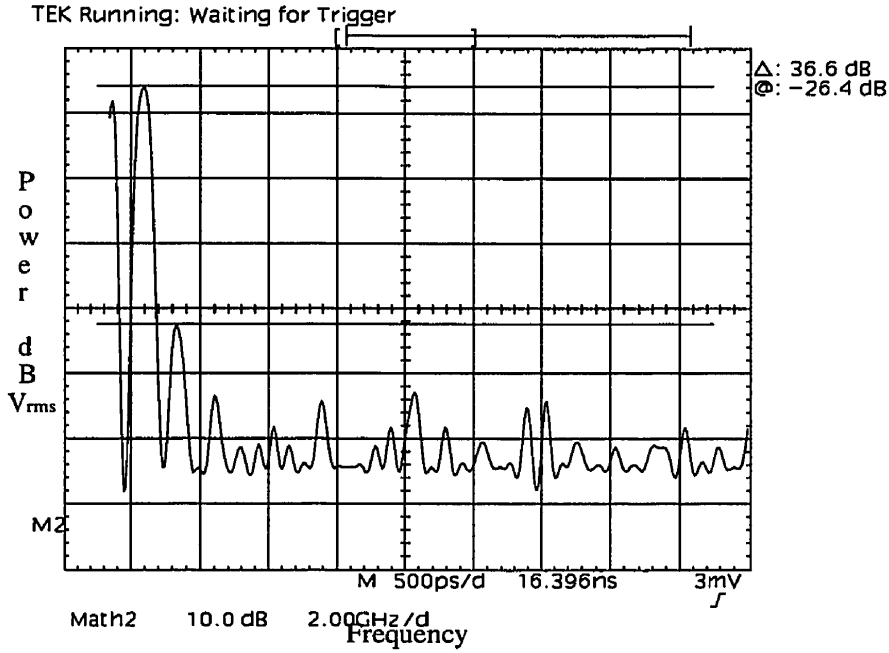


Figure 4.13 FFT of Ref2(in figure 4.10)

Table 4.1 Distortion Measurements

Frequency:	1 GHz
Input:	-3.6 dBm
Output (max):	-13 dBm
HD_2:	-36.6 dB
HD_3:	-47.6 dB

Finally, the frequency response of the phase shifter is measured over a wide frequency range, with the same control sequence as that of figure 4.12. The response is plotted on figure 4.14. It can be seen from figure 4.14, that the circuit is usable from .7 to 1.5 GHz. A summary of the circuit specifications is shown in table 4.2.

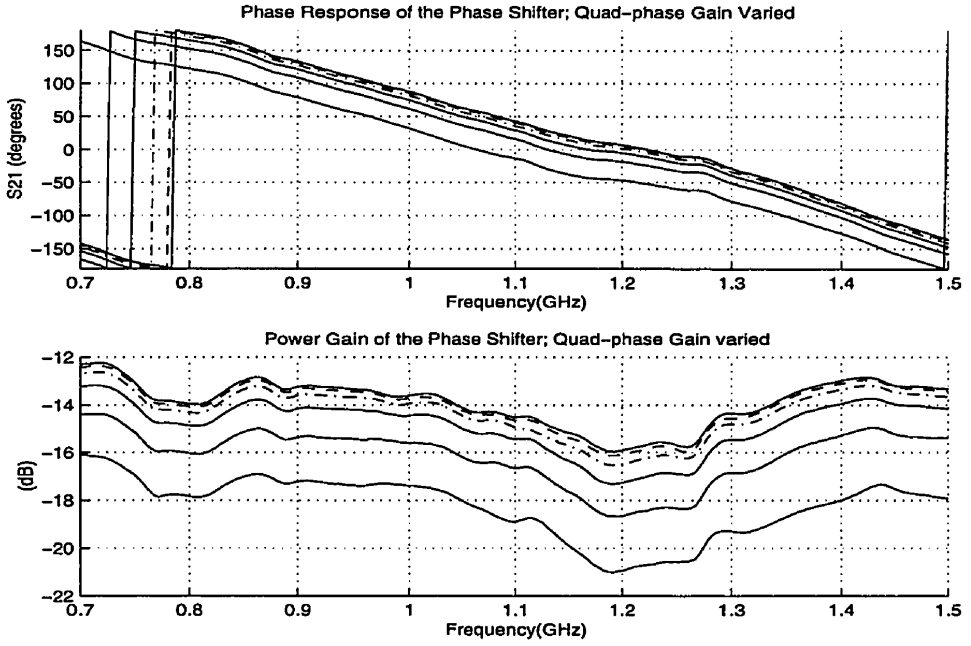


Figure 4.14 Frequency Range of the Phase Shifter

Table 4.2 Circuit Specifications

Technology:	0.8um BiCMOS
Power:	250mW @ 3.3V
Usable Bandwidth:	.7- 1.5 GHz
die size :	1.36x1.46 mm^2

CHAPTER

Conclusion

This chapter summarizes the contributions of the thesis, and outlines the directions for future work.

5.1 Thesis Conlusion

This thesis investigated the feasibility of using silicon bipolar homojunction transistor technology to realize a 1 GHz variable phase shifter. A monolithic variable phase shifter was realized in 0.8um BiCMOS technology. The circuit was tested and the phase response is close to simulation results. There are numerous possible applications for this circuit, one of them is for adaptive antennas. The silicon area required allows for 16 channels to be included in a single IC.

Chapter 1 presented different methods of realizing microwave electronic variable phase shifters. It also presented some applications for them.

Chapter 2 looked at some adaptive antenna structures and adaptation algorithms. It also showed the effects of finite weighting on the single-sidelobe canceller.

Chapter 3 presented the circuits that were used to realize the variable phase shifter. It presented a modified bandgap reference circuit.

Chapter 4 presented test results that prove the functionality of the circuit.

5.2 Future Work

Adaptive Antenna: Research is suggested on finding out whether it is more advantageous to weight the signal in RF, at an IF, or at baseband frequencies.

Programmable Phase Shifter: Since the motivation of the present work is for adaptive antenna applications in wireless communications, future work is suggested in increasing the operating frequency of the circuit, in order for it to work at the unlicensed and globally available spectrum of 2.4-2.5 GHz. For example, using a now readily-available 25 GHz silicon bipolar technology would allow for 2.5 times increase in signal frequencies. Work is also suggested in modelling the circuit and package impedances at high frequency in order to match external terminations.

Appendix A

This section derives the transfer function of the RC polyphase network shown in figure A.1.

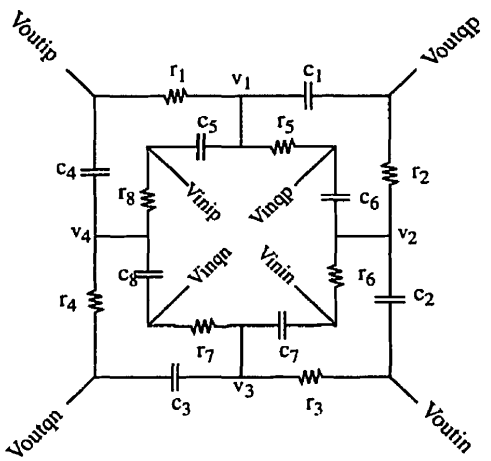


Figure A.1 RC Polyphase Network

We have the following set of equations:

$$(v_1 - Voutqp)gc_1 + (v_1 - Vinqp)g_5 + (v_1 - Voutip)g_1 + (v_1 - Vinip)gc_5 = 0 \quad \textbf{(a.1)}$$

$$(v_2 - Voutqp)g_2 + (v_1 - Vinqp)gc_6 + (v_2 - Voutin)gc_2 + (v_1 - Vinin)g_6 = 0 \quad \textbf{(a.2)}$$

$$(v_3 - Voutin)g_3 + (v_3 - Vinin)gc_7 + (v_2 - Voutqn)gc_3 + (v_1 - Vinqn)g_7 = 0 \quad \textbf{(a.3)}$$

$$(v_4 - Vinqn)gc_8 + (v_4 - Voutqn)g_4 + (v_4 - Vinip)g_8 + (v_4 - Voutip)gc_4 = 0 \quad \textbf{(a.4)}$$

$$(Voutip - v_1)g_1 + (Voutip - v_4)gc_4 = 0 \quad \textbf{(a.5)}$$

$$(Voutqp - v_2)g_2 + (Voutqp - v_1)gc_1 = 0 \quad \text{(a.6)}$$

$$(Voutin - v_3)g_3 + (Voutin - v_2)gc_2 = 0 \quad \text{(a.7)}$$

$$(Voutqn - v_4)g_4 + (Voutqn - v_3)gc_3 = 0 \quad \text{(a.8)}$$

Where $g_i=1/r_i$, $gc_i=sc_i$, $r_1=r_2= ... = r_8$, and $c_1=c_2= .. = c_8$. Solving for Voutip, Voutqp, Voutin, and Voutqn results to

$$Voutip = \frac{Vinin[src + 2(src)^2 + (src)^3] + Vinip[3src + 14(src)^2 + 3(src)^3]}{[1 + 4src + (src)^2][1 + 6src + (src)^2]} + \frac{Vinqn[5(src)^2 + 6(src)^3 + (src)^4] + Vinqp[1 + 6src + 5(src)^2]}{[1 + 4src + (src)^2][1 + 6src + (src)^2]} \quad \text{(a.9)}$$

$$Voutqp = \frac{Vinin[1 + 6src + 5(src)^2] + Vinip[5(src)^2 + 6(src)^3 + (src)^4]}{[1 + 4src + (src)^2][1 + 6src + (src)^2]} + \frac{Vinqn[src + 2(src)^2 + (src)^3] + Vinqp[3src + 14(src)^2 + 3(src)^3]}{[1 + 4src + (src)^2][1 + 6src + (src)^2]} \quad \text{(a.10)}$$

$$Voutin = \frac{Vinin[3src + 14(src)^2 + 3(src)^3] + Vinip[src + 2(src)^2 + (src)^3]}{[1 + 4src + (src)^2][1 + 6src + (src)^2]} + \frac{Vinqn[1 + 6src + 5(src)^2] + Vinqp[5(src)^2 + 6(src)^3 + (src)^4]}{[1 + 4src + (src)^2][1 + 6src + (src)^2]} \quad \text{(a.11)}$$

$$Voutqn = \frac{Vinin[5(src)^2 + 6(src)^3 + (src)^4] + Vinip[1 + 6src + 5(src)^2]}{[1 + 4src + (src)^2][1 + 6src + (src)^2]} + \frac{Vinqn[3src + 14(src)^2 + 3(src)^3] + Vinqp[src + 2(src)^2 + (src)^3]}{[1 + 4src + (src)^2][1 + 6src + (src)^2]} \quad \text{(a.12)}$$

For Vinin=-Vinip and Vinqn=Vinqp=0, the equations reduce to

$$Voutip = -Voutin = \frac{2src}{1 + 4src + (src)^2} Vinip \quad \text{(a.13)}$$

$$Voutqp = -Voutqn = \frac{-[1 - (src)^2]}{1 + 4src + (src)^2} Vinip \quad \text{(a.14)}$$

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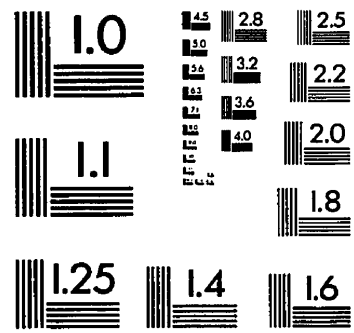

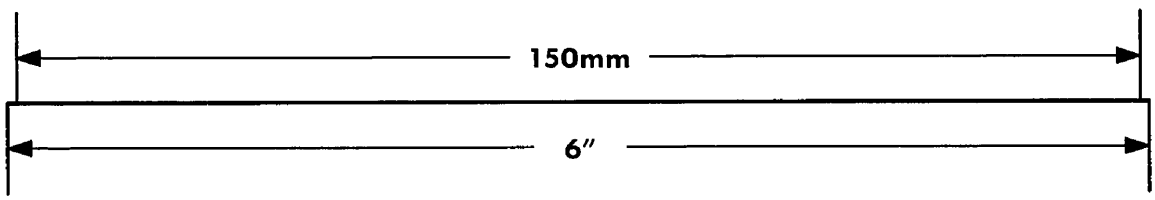

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